DOKUZ EYLÜL UNIVERSITY

GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

FABRICATION AND CHARACTERIZATION OF NANOMATERIAL BASED THIN FILM TRANSISTOR AND ADAPTABILITY TO DISPLAY TECHNOLOGIES

by

Çağlar ÖZER

February, 2022

İZMİR

FABRICATION AND CHARACTERIZATION OF NANOMATERIAL BASED THIN FILM TRANSISTOR AND ADAPTABILITY TO DISPLAY TECHNOLOGIES

A Thesis Submitted to the
Graduate School of Natural and Applied Sciences of Dokuz Eylül University
In Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy in Nanosicence and Nano Engineering,
Nanosicence and Nano Engineering Program

by

Çağlar ÖZER

February, 2022

İZMİR

Ph.D. THESIS EXAMINATION RESULT FORM

We have read the thesis entitled **"FABRICATION AND CHARACTERIZATION OF NANOMATERIAL BASED THIN FILM TRANSISTOR AND ADAPTABILITY TO DISPLAY TECHNOLOGIES"** completed by **ÇAĞLAR ÖZER** under supervision of **ASSOC. PROF. DR. M. FARUK EBEOĞLUGİL** and we certify that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Doctor of Philosophy.

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ACKNOWLEDGMENTS

I would like to express my sincere indebtedness and gratitude to my thesis advisor Assoc. Prof. Dr. M. Faruk EBEOĞLUGİL for all his time and effort. His guidance and contribution at every stage of my work really helped me to complete this work. Also, I would like to thank to Prof. Dr. Korkut Yeğin and Assoc. Prof. Dr. Mustafa Erol for his helpful suggestions at the periodic meetings of this research.

Additionally, I would like to thank to Assist. Prof. Dr. Serdar Yıldırım for leading the creation of this study. I would also like to thank my dear friends Sevcan Kardelen and Neslihan Şakar, who supported me throughout the thesis period.

I would like to express my endless respect and thanks to Mr. Metin Nil (Project and Incentive Group Manager, VESTEL) and Mr. Kıvanç Karslı (Optical Design Group Manager, VESTEL), who have always supported and motivated me to complete this work.

At the same time, I send my love and respect to all VESTEL, Optical Design Group employees who have supported me throughout this work.

Synthesis and characterization measurements performed at Dokuz Eylul University, The Center for Fabrication and Applications of Electronic Materials. This research was fully supported by Vestel Electronics and The Scientific and Technical Research Council of Turkey (TUBITAK) under Project No. 3180395. Special Thanks to VESTEL Electronics for their kind and continuous support.

Finally, I would like to thank my parents who have supported me all the way since the beginning of my studies. Their love gave me forces to make this work.

Çağlar ÖZER

FABRICATION AND CHARACTERIZATION OF NANOMATERIAL BASED THIN FILM TRANSISTOR AND ADAPTABILITY TO DISPLAY TECHNOLOGIES

ABSTRACT

In this study, ITO-coated PET was used as the substrate to create a flexible and transparent structure. a-IGZO (amorphous $InGaZnO_4$) is preferred for the semiconductor layer in order to keep the related TFT device stable at high performance for a long term. In addition, as an innovative method to increase the electrical performance of this TFT, the HfO_2 dielectric layer surface has been modified with $SrTiO_3$. All layers of the relevant flexible transparent thin film transistor (TTFT) structure were produced by the sputtering method. In this work, fabricated TFT devices were evaluated in terms of the structural, morphological, chemical and optical properties using X-ray diffraction (XRD), scanning electron microscope (SEM), atomic force microscopy (AFM), X-ray photoelectron (XPS) and UV-VIS spectroscopy, respectively. In addition, in order to examine the long term electrical performance of the related TFT devices, the relevant products were put into the reliability tests for TV panel production market and their electrical performances before and after the tests were determined. The average optical transmittance values of the developed TFT devices in visible range of electromagnetic spectrum were determined as percentage of 79.80. After the reliability tests, it was determined that there was a negligible decrease in the fet mobility value of the device. The fact that the fet mobility value is so high after long-term stability tests shows that the relevant flexible and transparent TFT device can be used to drive LC (liquid crystal) and OLED (organic light emitting diode) subpixels in LCD and OLED screen technologies.

Keywords: Flexible and transparent electronic, a-IGZO, TTFT, reliability, high K oxide, high fet mobility

NANOMALZEME TABANLI İNCE FİLM TRANSİSTÖRÜN ÜRETİMİ VE KARAKTERİZASYONU VE EKRAN TEKNOLOJİLERİNE UYARLANABİLİRLİĞİ

ÖZ

Bu çalışmada, ITO kaplı PET esnek ve şeffaf bir yapı oluşturmak için alttaş olarak kullanıldı. A-IGZO (amorf $InGaZnO_4$), ilgili TFT cihazının uzun süre yüksek performansta stabil kalması için yarı iletken katman olarak tercih edilmiştir. Ayrıca, bu TFT'nin elektriksel performansını artırmak için yenilikçi bir yöntem olarak, HfO_2 dielektrik katman yüzeyi $SrTiO_3$ ile modifiye edildi. İlgili esnek şeffaf ince film transistör (TTFT) yapısının tüm katmanları, püskürtme yöntemiyle üretildi. Bu çalışmada üretilen TFT cihazları sırasıyla X-ışını kırınımı (XRD), taramalı elektron mikroskobu (SEM), atomik kuvvet mikroskobu (AFM), X-ışını fotoelektron (XPS) ve UV-VIS spektroskosi kullanılarak yapısal, morfolojik, kimyasal ve optik özellikleri açısından değerlendirilmiştir. Ayrıca ilgili TFT cihazlarının uzun dönem elektriksel performanslarının incelenmesi amacıyla ilgili aygıtlar TV panel üretim pazarına uygun güvenilirlik testlerine tabi tutulmuş ve test öncesi ve sonrası elektriksel performansları belirlenmiştir. Geliştirilen TFT cihazlarının elektromanyetik spektrumun görünür aralığındaki ortalama optik geçirgenlik değerleri yüzde 79.80 olarak belirlendi. Güvenilirlik testleri sonrasında cihazın fet mobilite değerinde ihmal edilebilir bir azalma olduğu tespit edildi. Uzun süreli stabilite testlerinden sonra fet mobilite değerinin bu kadar yüksek olması, ilgili esnek ve şeffaf TFT cihazının LCD ve OLED ekran teknolojilerinde LC (sıvı kristal) ve OLED (organik ışık yayan diyot) alt piksellerini sürmek için kullanılabileceğini göstermektedir.

Anahtar kelimer: Esnek ve şeffaf elektronik, a-IGZO, TTFT, güvenilirlik, yüksek κ oksit, yüksek fet mobilitesi

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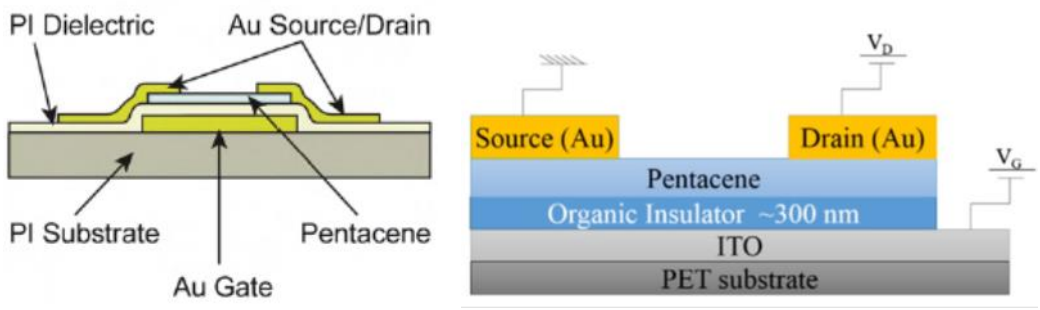
CHAPTER ONE

INTRODUCTION

1.1 General

The use of a flexible and transparent substrate material in a thin film transistor structure, the relevant layers being transparent for the visible area and the thin films to be formed on this substrate will allow the thin film transistor structure to be used in both flexible and transparent electronic applications.

When the studies in the literature are examined, it is seen that it is necessary to use a flexible substrate in order to produce a flexible thin film transistor. In this context, the most used substrate types in the literature are Kapton Pl films, PC (Poly Carbonate) films, PES films and ITO-coated PES and PET films (Carlos et al., 2017; He et al., 2011; Hsu et al., 2013; Kim et al., 2013; Ko et al., 2011; Liu et al., 2018; Park et al., 2009; Xu et al., 2018). Kapton, PC and PES (PES pads without ITO coating) film pads are not produced with a conductive film layer such as ITO, so a separate coating must be applied on these pads for the gate contact of the thin-film transistor. Since ITO coated PES or PET pads can be commercially available with a conductive film layer such as ITO on them, there is no need for a separate coating for the gate contacts of the thin-film transistor in studies where these types of commercial products are used as flexible pads (See fig.1).



(A) (B)

Figure 1.1 Thin-film transistor structures using a) Kapton Pl film (Park et al., 2009) and b) ITO-coated PET film (Carlos et al., 2017) as a substrate

In addition, the conductive contacts to be used in transparent electronics applications must be able to transmit the rays in the visible region to a great extent. In this context, the use of ITO-coated PET films as a substrate in flexible transparent thin film transistor structures comes to the forefront due to its commercially available, affordable prices, good light transmission in the visible range and the advantages it will bring in application.

By using different types of dielectric materials in TFT structures, it is possible to operate these structures at different operating voltages and frequencies (Chen et al., 2014; Choi & Song, 2018; Han et al., 2018; Jo et al., 2018; Lee, Shin, et al., 2017; Meena et al., 2011; Ozer et al., 2022; Salvatore et al., 2014). Thus, the possibility of using these TFT structures in different electronic applications emerges (Branquinho et al., 2014; Lee, Jeong, et al., 2017; Lim et al., 2013; Nakano et al., 2012; Park et al., 2009; Rim et al., 2014; Rim et al., 2017). However, rapid developments in metal oxide semiconductor integrated circuits (CMOS ICs) have made significant contributions to the consumer electronics and microelectronics industry (He et al., 2011; Robertson & Wallace, 2015).

SiO_2 has been the most preferred dielectric material in CMOS IC structures since it can preserve its dielectric properties quite well at the interface formed with single crystal silicon even in its natural oxide form (Liu et al., 2018; Ozer et al., 2022). In addition to all these, the increase in demand for high performance despite acceptable power consumption values for many electronic devices today necessitated a significant reduction in the size of electronic devices such as field effect transistors (FETs) used in CMOS IC structures (Liu et al., 2018; Ozer et al., 2022). At this stage, the relative thickness of the SiO_2 layer decreases towards atomic levels together with the dimensions of the relevant transistor structures used as dielectric structure, causing the Gate leakage current density values of these transistor structures to increase significantly (See figure 1.2). In this case, it causes large increases in the power consumption values of electronic devices, especially in standby mode, where the relevant transistor structures will be used (Liu et al., 2018).

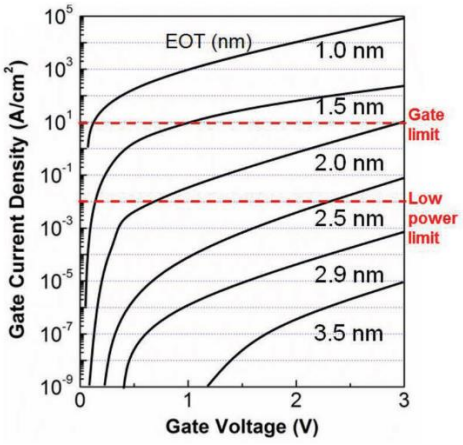


Figure 1.2 Change in gate leakage current values vs. different gate dielectric layer thicknesses (Liu et al., 2018)

If it is desired to reduce the power consumption of a TFT device while maintaining the current high performance, an improvement should be made in the existing dielectric layer. When equation 1.1 is examined, increasing the capacitance (C_i) value of the dielectric layer per unit area while preserving the related channel geometry (W/2L aspect ratio) of the TFT structure means that this TFT structure can pass the same I_{ds} currents at lower voltages. In this case, it means that the TFT structure works by maintaining its current performance by consuming less power.

$$I_{ds} = \frac{W}{2L}\mu C_i(V_g - V_{th})^2 \tag{1.1}$$

When equation 1.2 is examined in order to use a dielectric structure with a higher capacitance value per unit area in the TFT structure, the thickness, d, of the dielectric layer in the relevant TFT structure should be reduced and in addition to this, a higher dielectric constant (*k*) material should be used.

$$C = \frac{k\varepsilon_0 A}{d} \tag{1.2}$$

However, when thickness of dielectric material reduces the too much, the gate leakage current value of relevant TFT strucute will increases. This means that the power consumption of the electronic devices in which the relevant TFT structure is used will increase considerably, especially in the standby state. In this case, the most effective solution is to use dielectric materilas having high-k value, such as HfO2, on dielectric layer (Gutierrez-Heredia et al., 2017).

When the studies on thin film transistor applications in the literature are examined, modification of the interface between the dielectric and the semiconductor layers contributes positively to the increase of the electrical properties such as mobility of the thin film transistor structure (Kang et al., 2017; Ozer et al., 2022). In a study conducted by Kang et al. In 2017, they modified the surface of the SiO_2 dielectric layer by using TaOx dielectric material as a buffer layer between the SiO_2 dielectric layer and the IGZO semiconductor layer in the thin film transistor structure they produced and showed that this surface modification positively improved the mobility value of the transistor (See figure. 1.3 and table 1.1).

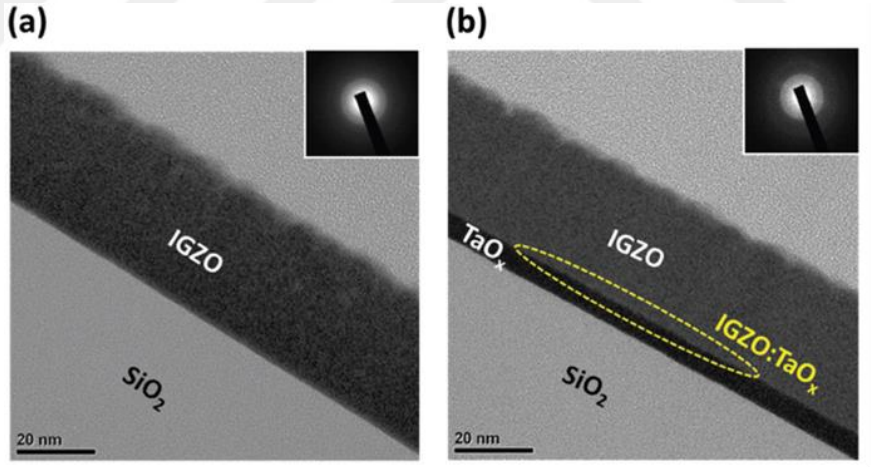


Figure 1.3 4nm thick TaOx layer - cross-sectional HR-TEM image (Kang et al., 2017)

Table 1.1 Effect of TaOx buffer layer having 0, 2nm, 4nm and 6nm thicknesses on the mobility values of thin film transistor (Kang et al., 2017)

Type of Sample	**μ_{sat} ($cm^2V^{-1}s^{-1}$)**	**V_{th} (V)**	**SS (V dec^{-1})**	**$I_{on/off}$**
Sample A	12.78 ± 1.03	-0.32 ± 0.42	0.57 ± 0.07	$\approx 10^7$
Sample B	15.91 ± 0.92	-0.18 ± 0.27	0.41 ± 0.03	$\approx 10^8$
Sample C	19.14 ± 2.41	-1.12 ± 0.18	0.23 ± 0.02	$\approx 10^8$
Sample D	23.11 ± 1.66	-12.56 ± 0.92	0.41 ± 0.03	$\approx 10^9$

When thin film transistor applications are examined, it is seen that metal oxide based semiconductor materials are frequently used in these applications to ensure long-term stability. Due to their high mobility values, ZnO, SnO_2 and In_2O_3 are some of these semiconductors. However, materials, such as ZnO, SnO_2 and In_2O_3, are semiconductor materials in polycrystalline structure. Polycrystalline materials have grain boundaries, and these boundaries are the regions where electrons are most likely to be trapped. Especially in large-scale applications, these grain boundaries increase and possibly cause the electrical properties of the electronic device such as mobility to decrease. This causes the current electronic device to operate with lower efficiency (Esro et al., 2015; Mativenga et al., 2015; Nomura et al., 2004; Ozer et al., 2022; Xiao et al., 2018).

Considering especially large-area applications such as display technologies, it is thought that a metal oxide semiconductor material such as IGZO, ZIO, ZTO and ZnON that can show semiconductor properties in amorphous state will provide greater benefits and effects in related applications (Gutierrez-Heredia et al., 2017; Heremans et al., 2016; Ozer et al., 2022; Xu et al., 2018).

Unlike polycrystalline materials, amorphous materials do not have grain boundaries, which means that the possibility of trapping electrons in the structure is eliminated for the same reason. In addition, it is much easier to produce ultra-smooth surfaces with amorphous structures compared to polycrytsalline materials, and the fact that these structures can be easily produced at very low temperatures has led these materials to be preferred in many applications, frequently (Hsu et al., 2013; Ozer et al., 2022; Xu et al., 2018). In addition to all these, due to the fact that some amorphous

oxide semiconductors such as IGZO are transparent, this feature makes them that the preferred choice for innovative consumer electronics applications such as transparent electronics (Aoki & Kunitake, 2004; Münzenrieder et al., 2015; Ozer et al., 2022; Xu et al., 2018).

As it is clearly seen in the studies in the literature, there is a TFT structure with low power consumption alone or a flexible and transparent structure alone. However, a TFT structure with all the features of low power consumption, flexibility and also transparency has not been developed to date. However, the fact that all layers of the TFT structure fabricated here will be developed with the same production method is one of the important advantages of this thesis. This will provide ease of mass production for the relevant TFT structure. Increasing the electrical properties of a TFT structure that provides low power consumption with the interface modification is another important advantage of the thesis. In addition, the fact that each layer of the TFT structure can be produced as amorphous makes the relevant TFT device suitable for large-area applications such as display technologies (Ozer et al., 2022).

1.2 Organization of the Thesis

In this thesis, a new generation flexible transparent thin film transistor (flexible transparent TFT) structure suitable for use in display technologies has been developed. ITO-coated PET has been used as a substrate in order to give the relevant structure flexible properties. High dielectric constant HfO_2 is used as the gate dielectric layer of the transistor structure to provide low power consumption in the structure. In addition, the interface between the gate dielectric layer and the semiconductor layer has been modified by coating with $SrTiO_3$ over the gate dielectric layer. Thus, the electrical performance of the existing TFT structure has been improved. IGZO, which is an amorphous oxide semiconductor, was used for semiconductor layer for concerning flexible transparent TFT structure to work stably in the long term. Another reason for preference is that IGZO has a high mobility value and can be produced transparently. All layers of the TFT structure are produced with the sputtering method, which is also suitable for large area production. Whether the structure can be produced as amorphous after production was determined by X-Ray Diffraction (XRD) analysis. Surface topographies and surface roughness values of the relevant layers were

determined by Atomic Force Microscopy (AFM) analysis. In addition, it was determined by X-Ray Photoelectron Spectroscopy (XPS) analysis that the produced layers have the correct chemical stoichiometry.

The mechanism that caused the improvement of electron mobility as a result of modification at the interface between the gate dielectric layer and the semiconductor layer was explained by XPS depth analysis. In order to show that the relevant TFT structures may work stably in the long term, relevant TFT devices have been subjected to thermal cycle test (TCT), thermal shock test (TST) and high temperature high humidity (HTHH) tests, which are important environmental reliability tests for screen technologies. The electrical measurements of the developed flexible transparent TFT devices were made before and after the tests and it has been shown that these new generation TFTs developed within the scope of this thesis can work stably in the long term with their superior electrical properties.

This thesis consists of five chapters. In the first chapter, general information about the related substrate and layer requirements for flexible and transparent TFT structures, which is the scope of this thesis, is given, examples from the studies in the literature regarding these structures are shown and the purpose of the thesis is mentioned. In the second part, general structure of TFTs, their working principles, general structures and application areas of new generation flexible and transparent structured TFTs are mentioned. In the third chapter, all detailed information about fabrication and characterization methods are given. In the fourth chapter, the results of all experimental activities of the developed flexible transparent TFT structure are given and these results are interpreted. In the fifth chapter, the conclusion and future plans are explained.

CHAPTER TWO

THEORETICAL BACKGROUND

2.1 Introduction to TFT Devices

With the developing technology, the need for low cost and low power consumption in electronic applications has gradually increased. In this context, researchers have carried out various studies on transistors, which are the building blocks of electronic devices. Thin film transistors (TFTs) using nanotechnological production processes can meet low cost demands due to their production methods. In addition, the fact that more transistor structures can be created per unit area has enabled the same electronic performance to be achieved with lower power consumption. Display technologies are among the main applications of TFTs. Many TFT types with different structures are currently used in backplain options of liquid crystal displays (LCDs) and OLED displays (Barquinha et al., 2012b).

A wide variety of studies on various materials and production methods for each layer forming TFTs have been extensively studied since the 1960s. Today, various TFT structures are used in many display applications from low-sized and low-cost TVs to large-sized, high-resolution, flexible and transparent TVs (Barquinha et al., 2012b).

With the developing technology, many different studies are carried out on TFTs in order to provide high performance in TVs with low power consumption, to ensure that TVs operate more stable in the long term, and to produce TVs in a flexible and transparent structure with innovative approaches (Barquinha et al., 2012b).

2.1.1 Device Structures of TFTs and Operations

TFTs that are a type of field effect transistor used to determine the value of the current to flow through a semiconductor located between the source-drain electrodes by adjusting the gate voltage. A dielectric layer is placed between the semiconductor layer and the gate electrode to provide current modulation in the TFT device. By changing the potential difference of the gate electrode, capacitive injection of carriers can be realized in the interface region between dielectric and semiconductor, and thus current modulation can be achieved (Barquinha et al., 2012b).

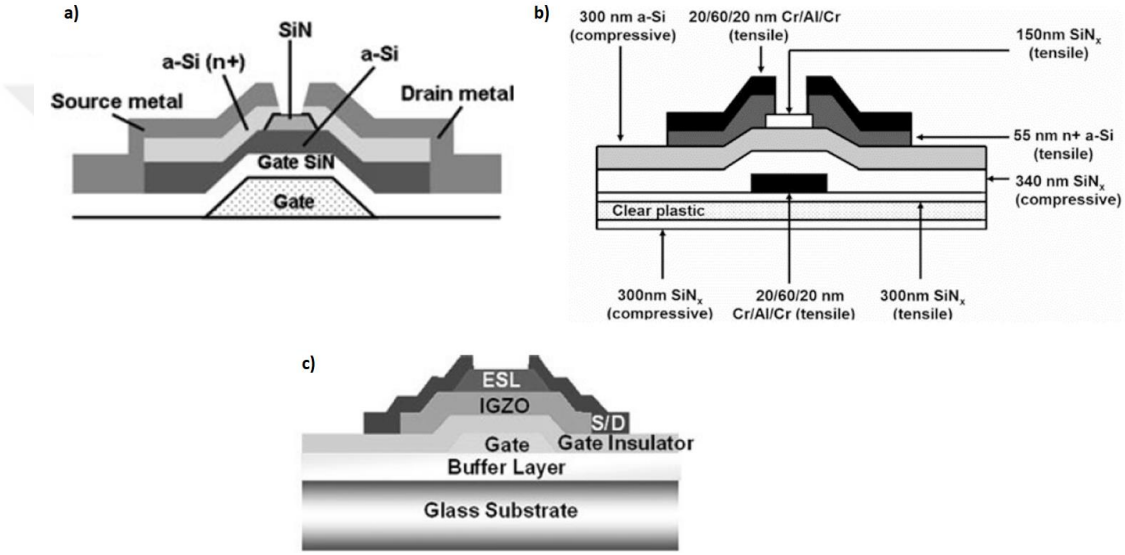


Figure 2.1 Schematic representation of different TFT structures a) Rigid TFT (Brotherton, 2013e), b) transparent TFT (Mo et al., 2011), c) flexible TFT (Cherenack et al., 2007)

In the TFT structures shown in Figure 2.1, it is possible to develop the TFT device in a transparent, flexible or both transparent and flexible structure by using different substrate, dielectric layer, semiconductor layer and electrode materials (Barquinha et al., 2012b). In addition, it is possible to develop energy-saving devices by using new generation dielectric layer and semiconductor materials in TFT structure (Barquinha et al., 2012b).

TFT devices can be produced as n type and p type (Barquinha et al., 2012b). The working principle of an ideal n type TFT device depends on the ability to provide electron transfer at the interface between the dielectric and the semiconductor layers. For this, the gate voltage (V_G) value of the TFT must be higher than the threshold

voltage (V_T) value that can achieve a downward band bending at the interface in the region close to the semiconductor layer. In practice, threshold voltage of a real TFT device deviates from 0 V depending on a function of the gate electrode-semiconductor work function difference, the semiconductor background carrier concentration, the charge density residing within the dielectric and the trap density at the interface and semiconductor (Barquinha et al., 2012b; M. Kim et al., 2007; Sato et al., 2009).

For $V_G>V_T$, when drain voltage of the TFT has positive, drain current (I_D) will flow between drain and source electrodes of TFT. For $V_G<V_T$, regardless of the value of V_D, the upward band bending at the interface between the semiconductor and the dielectric layer is negligible, and in this case the I_D current has very small values in the off state of the respective TFT device. TFTs have different on-state operation regime depending on the V_D voltage. These operation regimes are shown below.

- Pre-pinch-off regime (For $V_D<V_G–V_T$) (Barquinha et al., 2012b):

$$I_D = C_i \mu_{FE} \frac{W}{L}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2\right] \quad (2.1)$$

C_i is the gate capacitance per unit area, μ_{FE} is the field-effect mobility, W is the channel width and L is the channel length of TFTs. For very low V_D, the quadratic term can be neglected and in this case, a linear relation between I_D and V_D occurs that is known as linear regime of TFT devices.

- Post-pinch-off (saturation) regime (For $V_D>V_G–V_T$) (Barquinha et al., 2012b):

$$I_D = C_i \mu_{sat} \frac{W}{2L}(V_G - V_T)^2 \quad (2.2)$$

μ_{sat} parameter in equation 2.2 is called saturation mobility of TFT. In the saturation regime, the semiconductor layer near the drain region of the TFT is depleted. This phenomenon leads to saturation of I_D of related TFT and is called as pinch-off regime.

The output and transfer characteristics shown in Figure 2.2a and b are used to determine the operating parameters of TFT devices.To determine output characteristics, TFT is swept on V_D voltage for different V_G values. Different qualitative features from the output characteristics of TFTs can be obtained.

For example, a decreasing separation between I_D–V_D curves with increasing V_G is indicative of μ degradation for that V_G range. Good saturation level is a very important property, especially in circuits where TFT devices are used as electronic current limiters. (Barquinha et al., 2012b).

The low V_D region (linear regime region) also allow useful information about contact resistance between regarding layers for TFTdevices (Barquinha et al., 2012b).

To determine transfer characteristics of TFTs, TFT is driven on V_G voltage for constat V_D values. Different qualitative properties from the transfer characteristics of TFTs can be obtained. These useful parameters for TFTs:

- On/off ratio: This value is as the ratio of the maximum I_D current to the minimum I_D current. The min. I_D current usually depends on the noise level of measurement systems or the gate leakage current (I_G) value of the TFT. The maximum I_D value depends on the channel geometry, semiconductor layers in the TFT and efficiency of the capacitive charge injection. On/off ratio value in TFTs is usually above 10^6. However, for the successful usage of TFTs as electronic switches, On/off ratio should have a large value (Barquinha et al., 2012b).

- V_T and turn-on voltage (V_{ON}): In the previous section, it was indicated that V_T is related to the accumulation or conductive region that V_G value can create at the interface between dielectric layer and semiconductor layer. For an n-type TFT, depending upon whether V_T is positive or negative, TFTs can be operated on enhancement or depletion mode, respectively ((Hoffman et al., 2003). V_T can be determined by the linear extrapolation method of the I_D-V_G plot (for low V_D) or the $I_D^{1/2}$-V_G plot (for high V_D) (Ortiz-Conde et al., 2002).

- V_{ON}, on the other hand, is defined as the V_G value where the I_D value starts to rise in the log I_D-V_G graph, with its most common use in the literature (Hoffman, 2004).

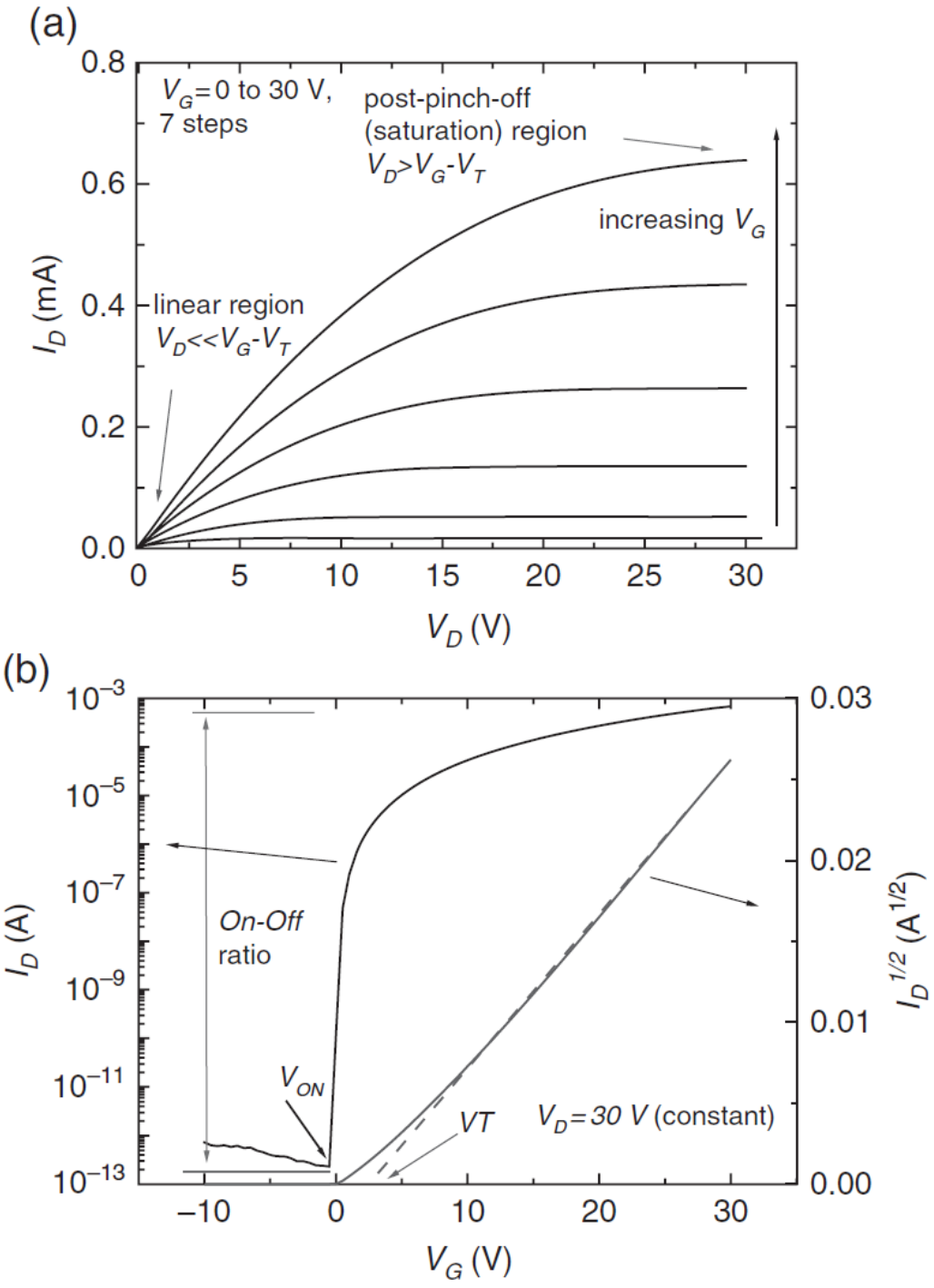


Figure 2.2 Typical electrical characteristics of n-type oxide TFT a) output and b) transfer characteristic

- Subthreshold swing (S): The inverse of the maximum slope in the transfer curve of TFTs remarks the VG voltaje that required to increase the ID value by one decade.

$$S = \left(\frac{d log(I_D)}{dV_G} \Big|_{\max I_D} \right)^{-1} \quad (2.3)$$

S value usually has a value of less than 1 for TFTs.Small S values such as 0.10-0.30Vdec^{-1} mean higher operating speed and lower power consumption in TFTs (Barquinha et al., 2012b).

- Mobility (μ): This value is related to efficiency of the carrier transport of the semiconductor layer of the TFT, as well as directly affected by the maximum ID current and operating frequency that the TFT is driven (Barquinha et al., 2012b). On a TFT devices, Carriers move through a narrow region close to the dielectric/semiconductor interface (Barquinha et al., 2012b).

The mobility value of TFT can be calculated by the following methods (Barquinha et al., 2012b):

- Effective mobility (μ_{eff}) - This value can be calculated by using conductance (g_d) for low V_D as follows:

$$\mu_{eff} = \frac{g_d}{C_i \frac{W}{L} (V_G - V_T)} \quad (2.4)$$

- Field-effect mobility (μ_{FE}) - This value can be obtained by using transconductance (g_m) for low V_D as follows:

$$\mu_{FE} = \frac{g_d}{C_i \frac{W}{L} V_D} \quad (2.5)$$

- Saturation mobility (μ_{sat}) - This value can be determined by using transconductance for high V_D (for saturation regime of TFT) with following equation:

$$\mu_{sat} = \frac{\left(\frac{d\sqrt{I_D}}{dV_G} \right)^2}{\frac{1}{2} C_i \frac{W}{L}} \quad (2.6)$$

Each method shown here for determination of mobility value of TFT device has advantages and disadvantages. For example, although μ_{eff} is significantly associated with V_G, V_T must also be determined for this value and in this case, V_T is highly sensitive to contact resistance (low V_D). μ_{FE} does not need V_T value and it is easy to calculate by the derivative of transfer characteristics. Finally, μ_{SAT} does not require a V_T value and it is less sensitive to contact resistance.

Hoffman proposes two different methods that are average (μ_{avg}) and incremental (μ_{inc}) mobility of TFT devices in literature (Hoffman, 2004). First one gives valuable information about avg. value of all carriers that moves in the active channel of TFT device. Second one provides information regarding carrier transport by examine the mobility of carriers (Barquinha et al., 2012b).

2.1.2 Application Areas of TFTs

Along with the developing technology, high performance, reliability and stable behavior become more impontant to meet the sensitive and indispensable demands of many technological applications such as solar cells, flexible displays, radio frequency identification (RF-ID) cards and developing biomedical applications (Gelinck et al., 2004; Krebs et al., 2009; Lin et al., 2011; Liu et al., 2015; Park et al., 2009).

The most common application areas for TFTs are in display technologies. TFT-based technologies allow microfabrication of large-area applications such as Si semiconductor-based flat-panel displays (Gutierrez-Heredia et al., 2017). Transistors are embedded within the panel itself. TFTs reduce crosstalk between pixels and improve image stability. Today, LCD panels and OLED displays use this technology.

All modern high-resolution and high-quality electronic visual display devices use TFT-based active matrix displays (Brotherton, 2013f). AMOLED displays also contain a TFT layer for active-matrix pixel addressing of individual organic light-emitting diodes (Brotherton, 2013f).

In addition, different TFT structures are also used in transparent and flexible display applications(Gelinck et al., 2004; Gutierrez-Heredia et al., 2017; Hoffman et al., 2003; Nomoto et al., 2011; Nomura et al., 2004; Park et al., 2009; Sekitani et al., 2005; Xiao et al., 2018).

2.1.3 Dominant TFT Technologies

In this section, the prominent TFT technologies will be compared with each other according to their performance, stability, price and production process. a summary informations regarding oxide, a-Si:H, poly-Si and organic TFTs are shown in table 2.1.

Table 2.1 Prominent features for dominant TFT technologies and comparison with each other (Anthony et al., 2010; Brotherton, 1995; Kamiya et al., 2010; Sirringhaus, 2009; Street, 2009).

TFT features	**a-Si:H**	**poly-Si (LTPS)**	**Organics**	**Oxides**
μ ($cm^2V^{-1}s^{-1}$)	1 max	50 to 100	0.1 to 1	1 to 100
S ($Vdec^{-1}$)$^+$	0.4 to 0.5	0.2 to 0.3	0.1 to 1.0	0.1 to 0.6
Leakage current (A)	$\sim10^{-12}$	$\sim10^{-12}$	$\sim10^{-12}$	$\sim10^{-13}$
Reproducibility	High	Low	Low	High
TFT for AMOLEDs	4 to 5 masks	5 to 9 masks	Poor applicability	4 to 5 masks
Manufacturing cost	Low	High	Low	Low
Long term TFT reliability	Low	High	Low in air	High (forecast)
Yield	High	Low	High	High
Process temperature (°C)	~250	<550	RT	RT to 350
CMOS fabrication	Very low performance	Yes, not for large areas	Low performance	Yes and large areas

The most mature TFT technology in display application is a-Si:H based TFT devices. Studies have been conducted on this technology for more than 40 years. (Anthony et al., 2010; Brotherton, 1995; Kamiya et al., 2010; Sirringhaus, 2009; Street, 2009).

Even if Oxide TFTs did not have as mature technology as a-Si: H TFTs, however they quickly managed to move from the research phase to the production phase for display applications. The biggest advantage here is that existing methods used in LCD manufacturing technologies, for example the sputtering method used to produce top TCO electrodes of LCDs, can also be used in the production of oxide TFTs (Anthony et al., 2010; Brotherton, 1995; Kamiya et al., 2010; Sirringhaus, 2009; Street, 2009).

Beacause of poly-crystalline nature of Poly-Si, this semiconductor has a major disadvantage for large area applications of display technologies, due to the fact that it has low uniformity in large areas and low reproducibility which is one of the biggest disadvantages of the display technology. Unlike Poly-Si semiconductors, a-Si:H, organic and oxide semiconductors can be produced as amorphous and this structural feature makes these semiconductors suitable for large area deposition (Anthony et al., 2010; Brotherton, 1995; Kamiya et al., 2010; Sirringhaus, 2009; Street, 2009). Mostly p-type semiconductor is used as active channel layer in organic TFT structures. Although N-type OTFTs exhibit worse properties, they can be used for organic CMOS inverter production (Dzwilewski et al., 2010).

2.2 Various TFTs for Backplane Options of Displays

There are many different TFT types that can be used in the field of display technologies. Technological details of these TFT types will be explained in this section.

2.2.1 a-Si TFT: Low-end Display

It is shown the most common architectures of a-Si:H TFTs in figure 2.3a and b. In figure 2.3a, a TFT device having inverted staggered structure is shwon. Gate metal contact of TFT is located at bottom side. This TFT structure occurs silicon nitride gate dielectric layer and a-Si:H semiconductor layer is on top of gate dielectric. On the other hand, the TFT structure in Figure 2.3b has a-SiNx:H layer on top side of concerning TFT, unlike that in Figure 2.3a. (Brotherton, 2013e).

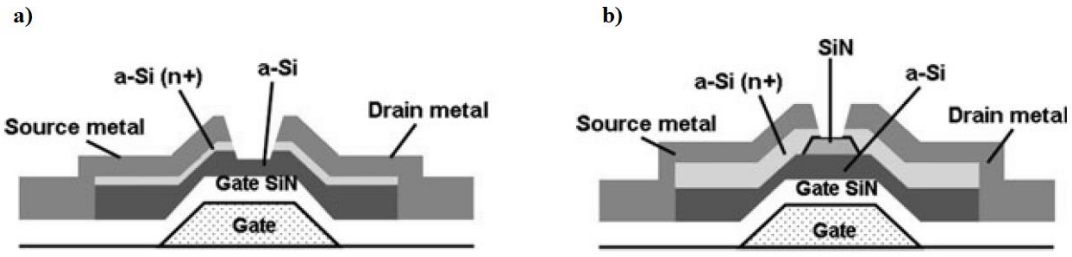


Figure 2.3 Inverted staggered a-Si:H TFT structures: (a) BCE and (b) ES architectures (Brotherton, 2013e)

To prevent dangling bond defects and improve deposition process of a-Si:H, hydrogen dopping has crytical importance for prodcution of a-Si:H. There are two different variations of this TFT structure. The variation often used in production is the back-channel-etched (BCE), TFT structure. The other variation for TFT structure is called the etch-stop (ES) and lots of research studies concerning this type of TFT structure are being in litrature. Both types of TFTs have similar layer structures. Although the BCE configuration requires a well-controlled etching procedure, it frequently is the preferred TFT structure in display technologies as it has a simpler manufacturing methods such as with fewer deposition and lithography steps. (Brotherton, 2013d).

The main layers of TFT such as gate dielectric layer and semiconductor layes, produce by plasma enhanced chemical vapour deposition (PECVD) system. This deposition system has a specific thermal process room that is called a parallel plate reaction chamber. Also, to created plasma in this PECVD system, there is a RF generator that is driven by 13.56 MHz. For he deposition process in PECVD system to fabricate above TFT structures, phosphine and ammonia doped silane gas is used, respectively. In addition, this primary reactant gas is diluted with hydrogen at a certain rate throughout the process and the bonding structures and electrical properties of the relevant layers are controlled (Brotherton, 2013d).

During the growth of the material, charge occupancy feature is used to specify these parameters: The position of the dangling bonds, DBs, energy level within the mobility gap. Using a-SiNx:H gate dielectric layer that has large positive charge density minimizes the effect of n-channel TFTs on the subthreshold slope. As a result of this

effect, α-SiNx:H is the most common gate dielectric in TFTs that has n-channel active layer. On the other hand, it provides poor performance for TFTs having p-channel active layer due to this DB location (Brotherton, 2013c).

Some of the important factors for TFTs to control on-state characteristics are FET mobility and threshold voltage values. The another important factors are semiconductor layer thickness and spreading resistance that occurs due to overlapping of gate, source and drain gate electrodes. For general TFT geometries in display technology, a-Si:H thickness as semiconductor layer is less than 200nm and overlapping value of gate, source and drain contacts is about 3μm. Also, according to some studies in literature, specific series resistance for TFTs having a-Si:H semiconductor layer can be effected major level by typical contact resistance of 0.25 Ωcm^2 (Brotherton, 2013c).

Another parameter that negatively affects the performance of the TFT is the leakage current value. Bulk condution contributes to TFT leakage current. This effect occurs by electron and hole conduction at the near interface of concerning layer in TFT. If the TFT device has high drain and high negative gate biases, this causes increasing leakage currents (Brotherton, 2013c).

Some results regarding the parameters affecting the series resistance effect, output characteristic and leakage current value of a-Si:H TFT are shared below.

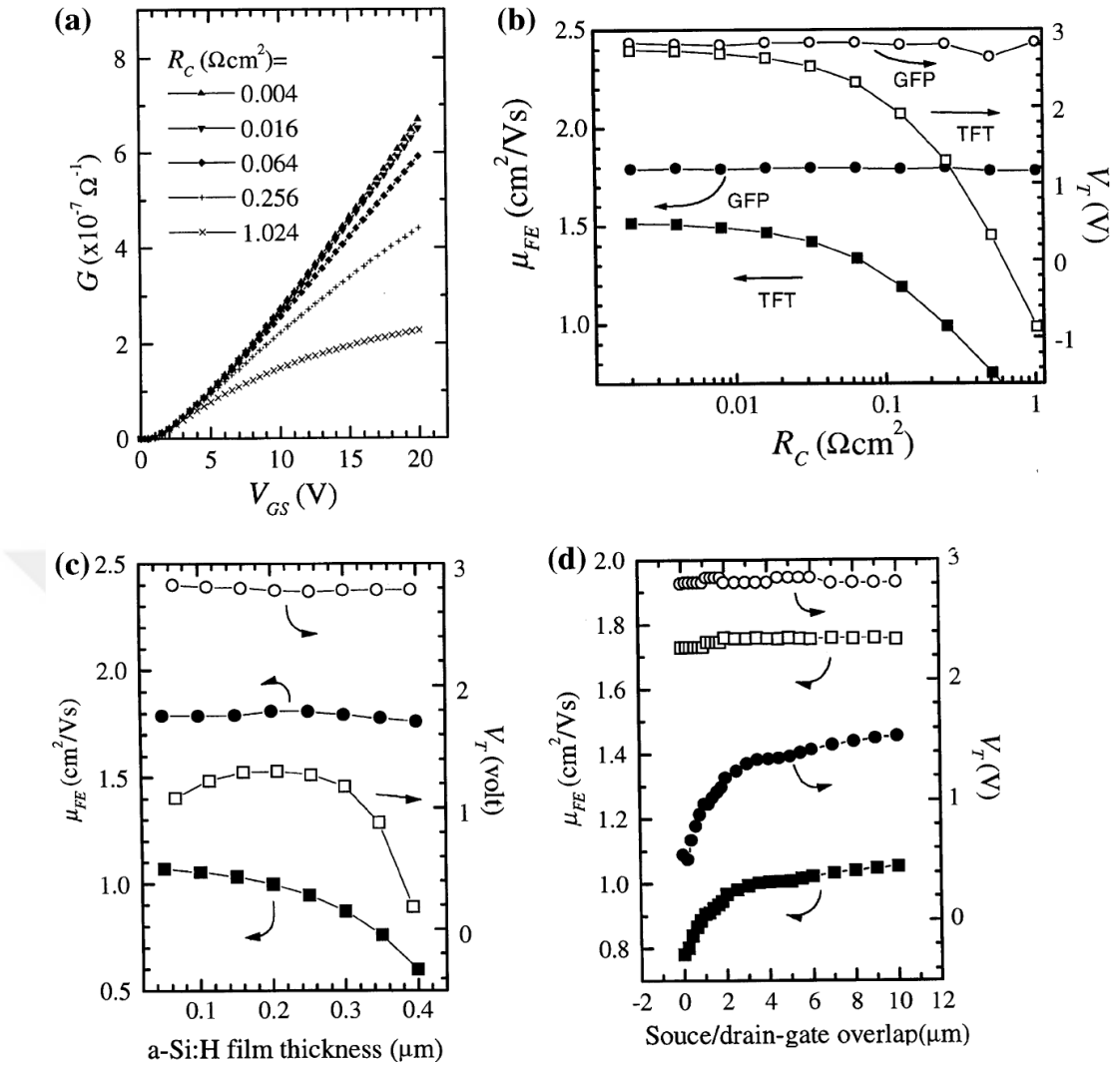


Figure 2.4 Series resistance effects for BCE and FGP TFTs (Simulation results) (Chen & Kanicki, 1997)

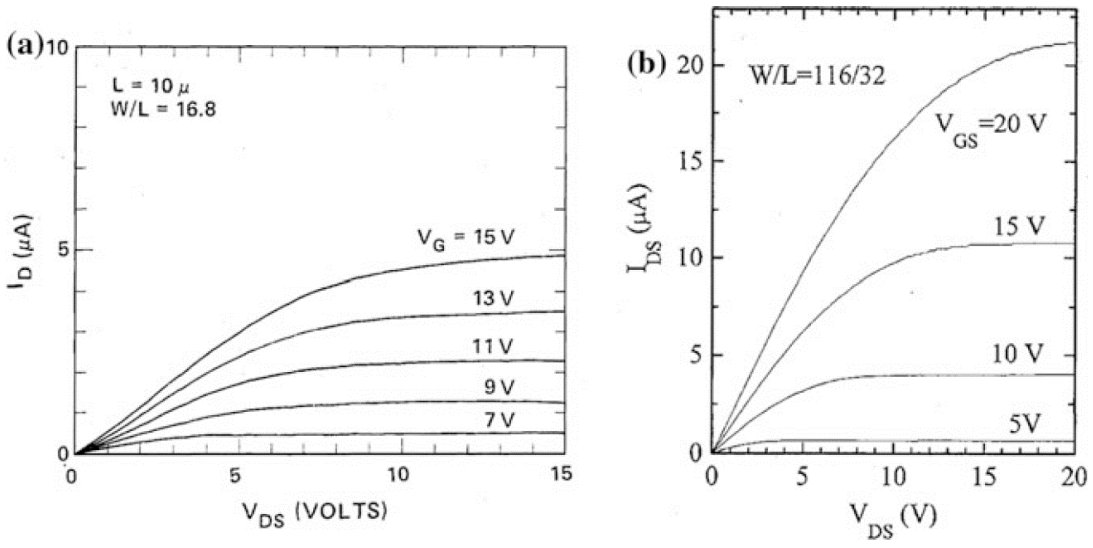


Figure 2.5 Output characteristics from two TFTs having different channel geometries a) At low drain bias (Chen & Kanicki, 1996) and b) Good quality contacts (Chen & Kanicki, 1996)

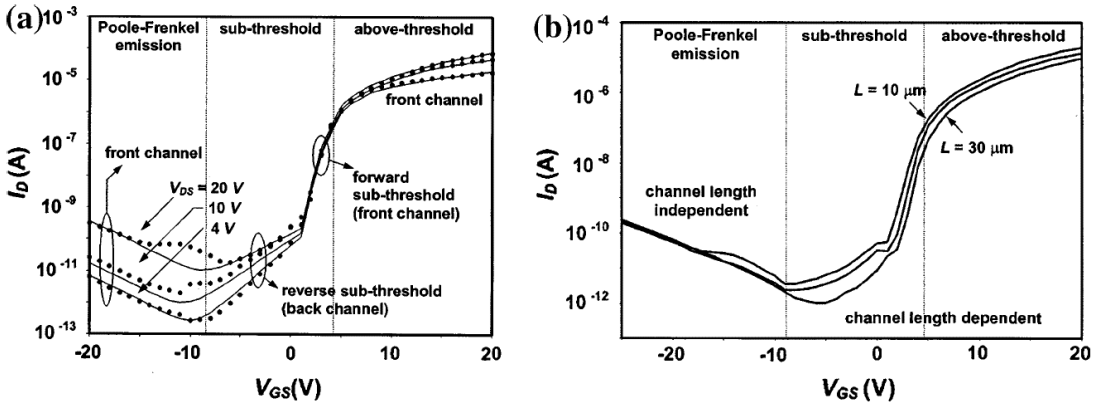


Figure 2.6 a-Si:H TFT transfer characteristics (Servati & Nathan, 2002)

2.2.2 LTPS TFT: High Performance and Resolution Display

NSA and SA configurations of the upper gate structure, which is the most common use of Poly-Si TFTs, are shown in Figure 2.7a and b, respectively (Gosain et al., 1995; Rohlfing et al., 2000). This TFT structure is different from the inverted staggered architecture. However, it is much more similar to SOI MOSFETs. Other similar points to SOI MOSFETs are that both n-channel and p-channel poly-Si TFTs with comparable performance can be produced by a common process. However, the same feature clearly distinguishes poly-Si TFTs from TFTs using organic or amorphous oxide materials.

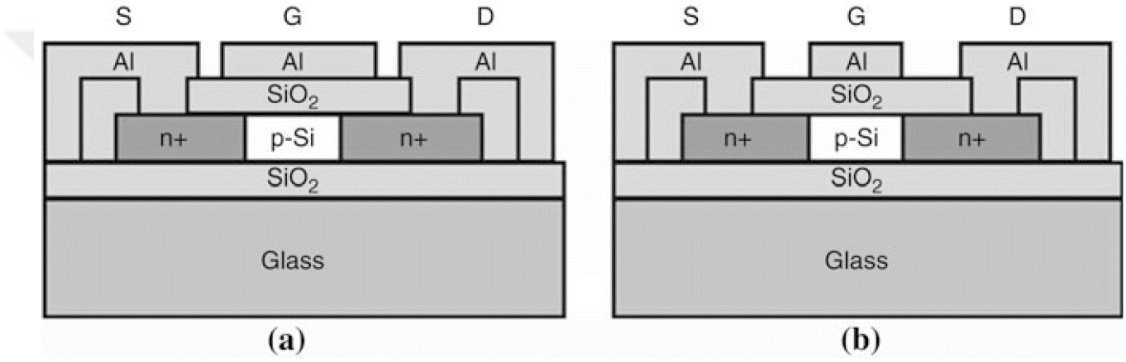


Figure 2.7 a) Non-self-aligned and (Rohlfing et al., 2000) b) self-aligned (Gosain et al., 1995) poly-Si TFTs

A-Si:H TFTs as backplain options were often used for large-scale production of AMLCDs in the early years of production. However, poly-Si soon gained great attention for TFTs as an innovative semiconductor active channel material. a-Si:HT TFTs have low carrier mobility, such as <1 cm^2/Vs and this is sufficient to address TFTs per pixel, however it can not provide the sufficient speed required for high screen refresh rate. Mobility of electron for Poly-Si TFTs has increased from <5 to ~120cm^2/Vs with routine manufacturing processes over the last 20 years, while innovative techniques that provide semi-crystalline-crystalline large-grain material have been able to be increased to ~ 900 cm^2/V (Mitani et al., 2008).

The higher carrier mobility offered by polycrystalline silicon contributes to the formation of second generation AMLCD technology. The displays (Harada et al., 2010) in which Poly-Si TFTs are integrated are currently small and medium size portable AMFPD, and they have entered mass production for AMFPDs. However, a-

Si: H TFTs continue to be the dominant AMLCD technology, especially for large size laptop, PC monitor and TV screens. Therefore, the current application of poly-Si TFTs is for small and medium size displays that make up ~ 36% of the AMLCD market (Brotherton, 2013b). In AMOLED market, this ratio is almost %100 especially for smart phones application (Brotherton, 2013b).

In addition to this, the level of integration of AMLCDs having poly-Si based TFT is expected to increase as more functionality regarding display backplain options is added to the panel side. (Harada et al., 2010). To obtain the higher circuit speeds, poly-Si TFTs have been improved to have higher mobility value and shorter channel lengths. These processes were carried out in accordance with the production on glass.

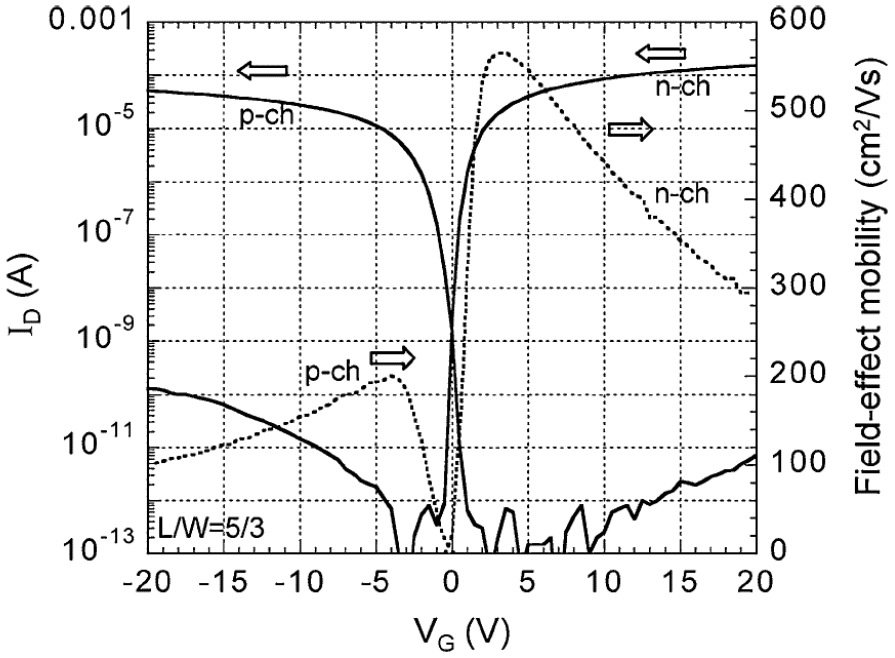


Figure 2.8 Transfer characteristics for TFTs with large grain crystallised by laser at 532 nm (Hara et al., 2002)

It is shown transfer characteristics of poly-Si TFTs in above figure 2.8. For Poly-Si TFTs, forming poly-Si thin films wiht laser crystallization are among the prominent production methods. Also, this directly influences carrier mobility and other main parameters of TFTs, such as threshold voltage and leakage current (Brotherton, 2013b). Figure 2.9 shows the relationship between the energy of the laser used for the crystallization process and the mobility value of the poly-Si TFT.

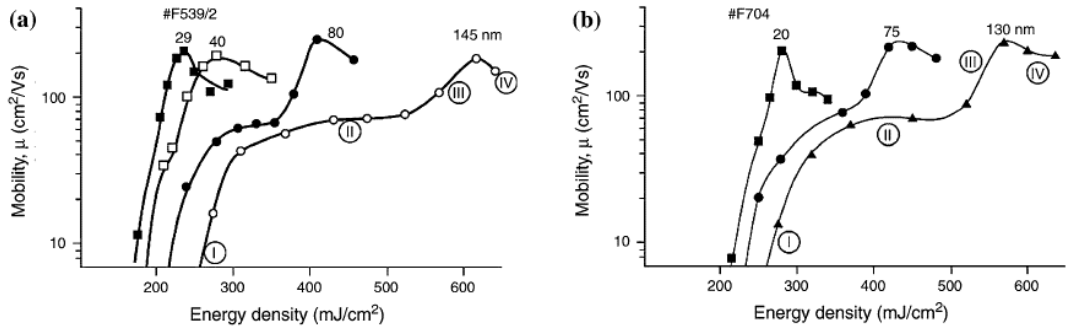


Figure 2.9 Electron mobility changing by a function of excimer laser energy density for different thickness a-Si films of a) KrF irradiation of LPCVD, b) XeCl irradiation of PECVD (Brotherton, 2013b)

Gate dielectric layer of poly-Si TFTs also influence threshold voltage and leakage current values. Therefore, the gate oxide in a TFT affects performance of the TFT device. The oxide materials that use in TFTs improve some properties. Low leakage current, low charges densities and interface states, high breakdown field, low pin-hole density, and good bias-stress stability features are some of these improved properties in TFT devices (Brotherton, 2013b).

2.2.3 OTFT: Lower Cost, Simple Fabrication Process

It started commercial interest for dispaly applications to organic TFTs (OTFTs) in the early 1990s. In the same period, carrier mobility in small molecule material, especially pentasin, passed over 0.1 cm^2/Vs and the mobility value of a-Si:H came close to 0.5-1.0 cm^2/Vs. The electrical performances of organic materials for OTFTs are increasingly improving and with large increases in carrier mobility over a 20-year time scale. As shown in Figure 2.10, the highest values currently exceed 10 cm^2/Vs (Brotherton, 2013a).

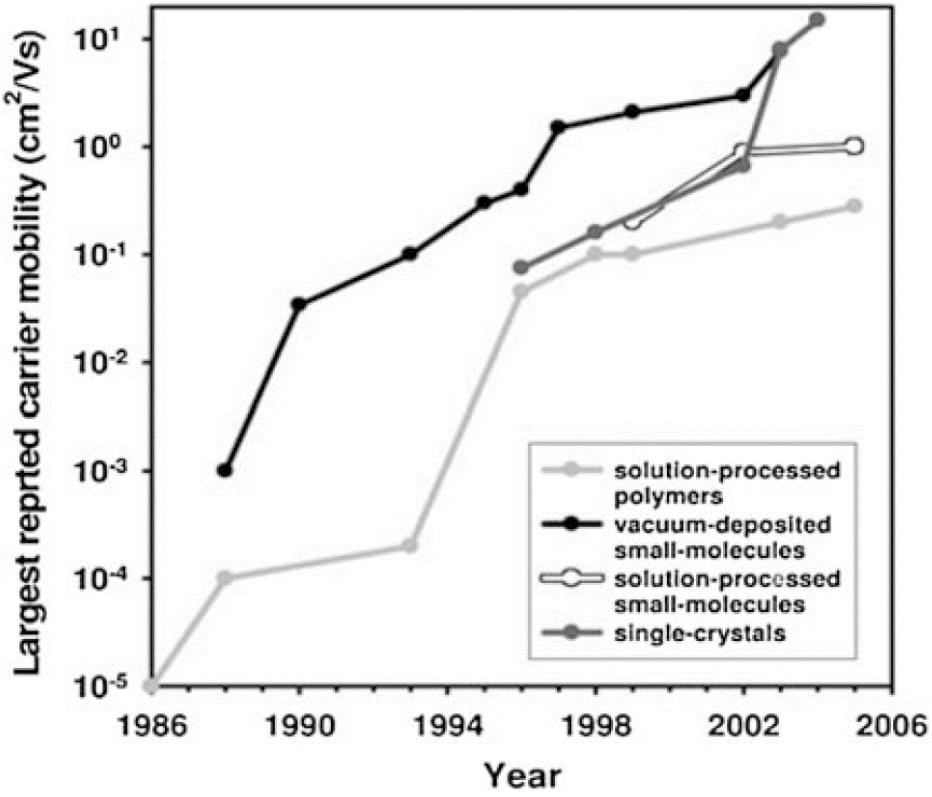


Figure 2.10 Carrier mobility changing for organic TFTs (Brotherton, 2013a)

Although, the current mobility values of organic materials are not sufficient to be considered as potential substitutes of a-Si:H. Therefore, organic semiconductıor based TFTs are unlikely to challenge a-Si:H TFT technology on glass in the near future. The studies of OTFTs has focused on a flexible substrate technology that uses inexpensive polymer substrates to produce lightweight, portable displays that can be shaped, folded or rolled. Some properties of polymer substrate OTFTs are shown in Table 2.

Table 2.2 Basic TFT performance parameters for some organic semiconductors (Brotherton, 2013b)

Material	**Channel**	**Gate Dielectric**	**Dielectric Thickness (nm)**	**Mobility (cm^2/Vs)**	**Threshold Voltage (V)**	**$I_{on/off}$ Ratio (log_{10})**	**SS (V/dec)**
P3HT	p	SiO_2 + HMDS	230	0.05-0.1	-	>6	0.44-0.65
PQT-12	p	SiO_2 + OTS	100	0.14	-	>7	1.5
Pentacene	p	SiO_2 + OTS	-	1.00	-5	7	-
DV Ant	p	SiO_2 + OTS	-	1.30	-16	7	-
TIPS-pentacene	p	SiO_2 + HMDS	370	0.65	3.4	8	0.14
PXX	p	PVP/OTS	400	0.40	-	7	0.17
Pentacene	p	AlO_x + SAM	-	0.50	-	>5	-
DNTT	p	AlO_x + SAM	6.3	0.60	-	6	-
$F_{16}CuPc$	n	AlO_x + SAM	-	0.01	-	>4	-
P(NDI2OD-T2)	n	PMMA	600-900	0.2-0.45	5-10	6-7	0.6-0.4
N3000	n	D2000	400-700	3.00	-	7	0.24-0.14

For inorganic TFT technologies, lots of researches in literature show that the maximum process temperature, the mismatch in the thermal expansion coefficients between the substrate and the layers on it, and the overall substrate stretch have important effects on the electrical characteristics of TFTs. However, these issues can be managed more easily in organic TFTs that can use more flexible substrates and have a better physical matched. For example, in the literature, applications with bend radius of 0.5 mm have been reported for suitably sealed OTFT samples placing TFTs (Sekitani et al., 2005) and as shown in Figure 2.11, it was shown applications with a bend radius of 4 mm as display (Nomoto et al., 2011).

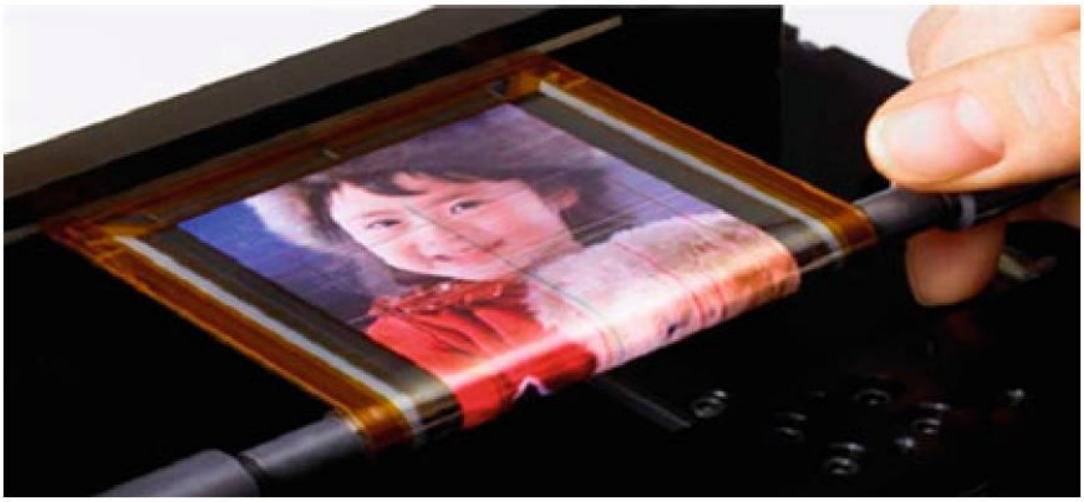


Figure 2.11 Rollable flexible AMOLED display (Nomoto et al., 2011)

Some of the examples of OTFT based on flexible substare is involved regarding LCDs (Sheraw et al., 2002), elecro-phoretic displays (EPDs) (Burns, 2012; Yoneya et al., 2012), OLEDs (Mizukami et al., 2006; Nakajima et al., 2009; Nomoto et al., 2011) and as well as demonstration logic circuits (Jeon et al., 2010; Klauk et al., 2007; Zschieschang et al., 2010). The other important applications for OTFTs are in low cost RFID tags and in AMEPDs. Some e-reader prototype that is aimed to produce a rollable/foldable screen have been presented (Burns, 2012; Yoneya et al., 2012). Also, various organic materials have been studied in the literature for OTFFs, both for the dielectric layer and related contacts, and for the semicondu-ctor layer (Brotherton, 2013a; Chen et al., 2012).

The most popular production methods used for OTFTs are spin coating (Dickey et al., 2006; McCulloch et al., 2006; Park et al., 2008), drop casting (Anthony et al., 2001; D. H. Kim et al., 2007; Lee et al., 2007), zone casting (Duffy et al., 2008) and inject printing (Guerin et al., 2011; Hong & Chung, 2012; Menard et al., 2007; Parashkov et al., 2005; Sele et al., 2005; Yun et al., 2011). Some of these methods is shown in figure 2.12. The most popular architectures used for OTFTs are shown in figure 2.13 (Chen et al., 2012).

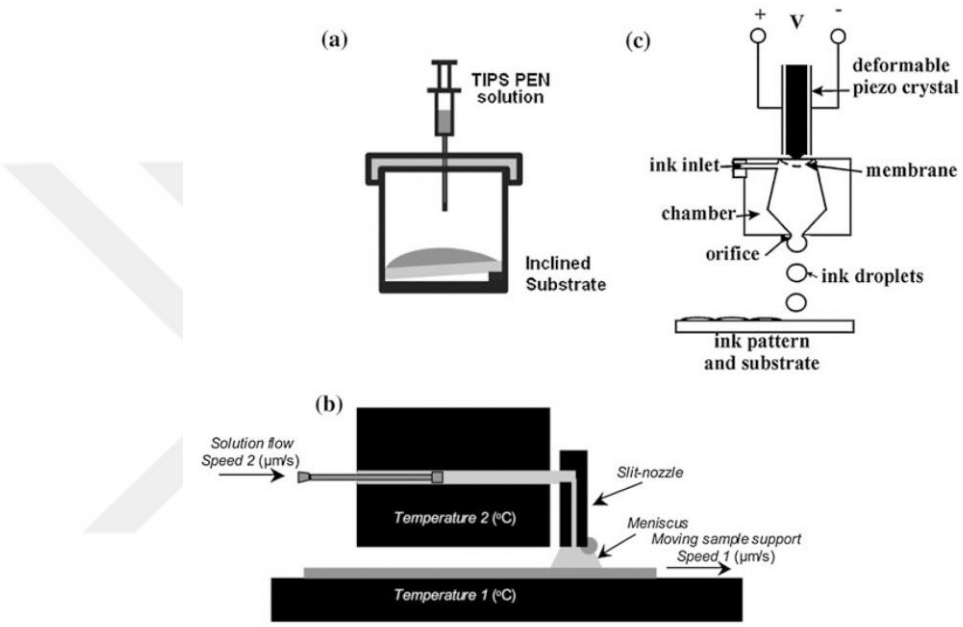


Figure 2.12 Fabrication methods for semiconductor films a) drop-casting (Lee et al., 2007), b) Zone-casting (Duffy et al., 2008), and (c) inkjet printing (Parashkov et al., 2005)

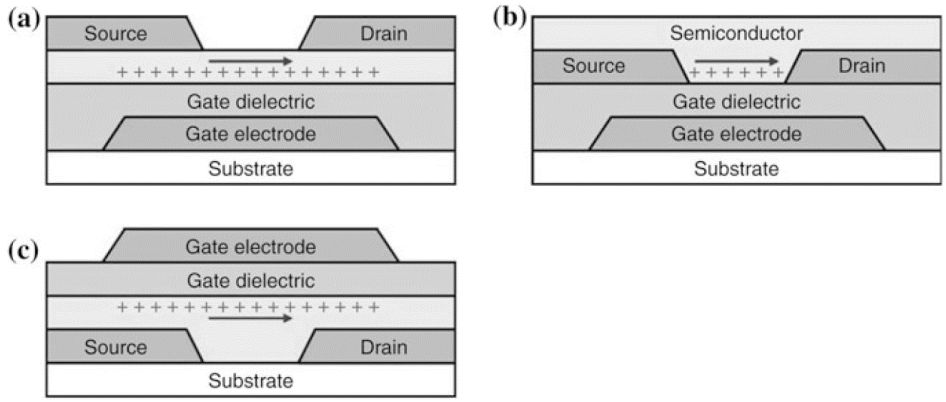


Figure 2.13 Different structures for OTFT device (Chen et al., 2012)

Contact and series resistance effects plays an important role to obtain overall TFT behaviour. In figure 2.14, it is clearly shown how bad contacts effect transfer and output characteristics of OTFTs (Hong et al., 2008; Kobayashi et al., 2009).

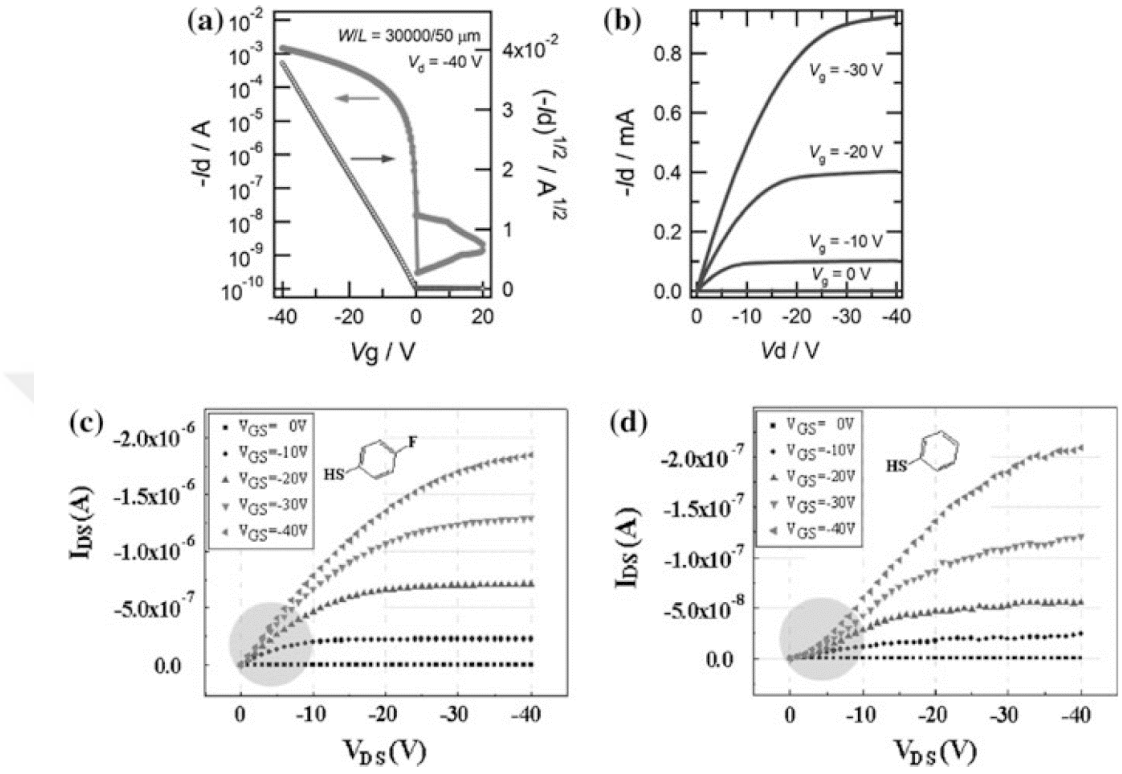


Figure 2.14 Electrical characteristics for Ph-PXX TFT a) transfer characteristics and b) output characteristics (Kobayashi et al., 2009).

As it is known, OTFTs are sensitive to moisture and oxygen, but studies on this issue are still ongoing (Yan et al., 2009). An example is shared in Figure 2.15 for the changing of the electrical performance of OTFTs in a humid environment.

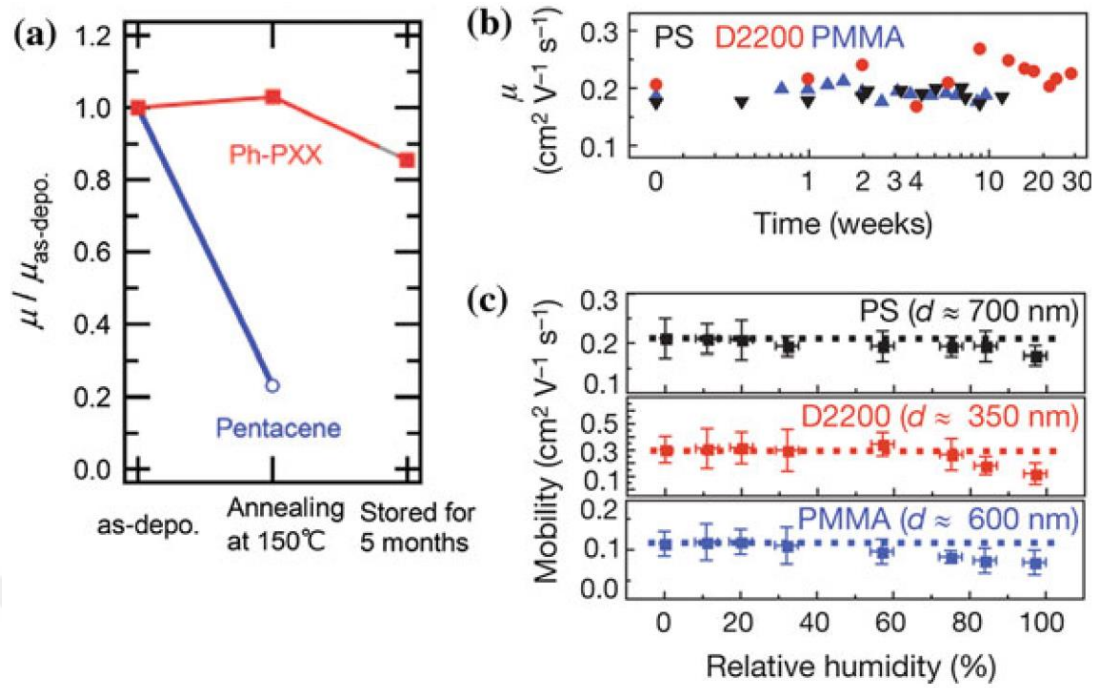


Figure 2.15 Comparison of some electrical parameters for pentacene and Ph-PXX TFTs (Kobayashi et al., 2009)

2.2.4 Amorphous Oxide TFT: Large-Sized Display

The current interest to amorphous oxide semiconductors (AOS) has started in 2004 with the TFT study with flexible polymer substrates that can be produced at low temperature using amorphous IGZO (Nomura et al., 2004). Since that time, lots of studies of active matrix displays addressed with a-IGZO TFTs on AOS have developed and have been tried in display technologies such as LCDs (Lu et al., 2012), OLEDs and electrophoretic e-readers (Ito et al., 2008).

The electron mobility value of this AOS material is ~10 cm^2/Vs, or more, which is <10 times higher than a-Si:H (Kamiya & Hosono, 2010). This value makes this material more suitable than a-Si:H for driving AMOLED displays. Considering that carrier mobility should be ~2 cm^2/Vs to drive diagonal >90 inch high resolution displays with 120 Hz, mobility value of AOS will be sufficient for high resolution AMLCDs (Hung et al., 2011; Kamiya & Hosono, 2010).

MP stage of large size and high resolution AMLCD TVs having AOS based TFTs has been guessed to begin in 2012 (Semenza, 2011). In addition, due to the nature of the amorphous structure, AOS TFTs can be produced more uniformly than poly-Si TFTs (Kamiya & Hosono, 2010). This situation has caused having AOS TFTs more interest than poly-Si TFTs that has high non-uniformity, in large-scale applications (Hung et al., 2011; Ito et al., 2008; Kamiya & Hosono, 2010). In addition to its high electron mobility value, its better general performance with a subthreshold slope of 0.12 V/dec value (Nomura et al., 2008) shows another superior aspect of AOS TFTs, when compared with 0.4 V/dec value of a-Si: TFT (Kuo et al., 2008).

When AOS TFTs are evaluated from the production point of view, they can be easily produced even at low temperatures such as room temperature with a system that has reached a certain technological maturity such as the sputtering method. Additionally, using wide range of dielectric materilas and simple contact metallisation process, they can be fabricated (Kamiya & Hosono, 2010).

The AOS TFT structure that is bottom gated, with either staggered (Arai et al., 2011; Osada et al., 2010; Seo et al., 2012) or coplanar (Lu et al., 2012; Osada et al., 2010) source and drain electrodes currently preferred in display applications is shown in Figure 2.16a and b, respectively (Osada et al., 2010).

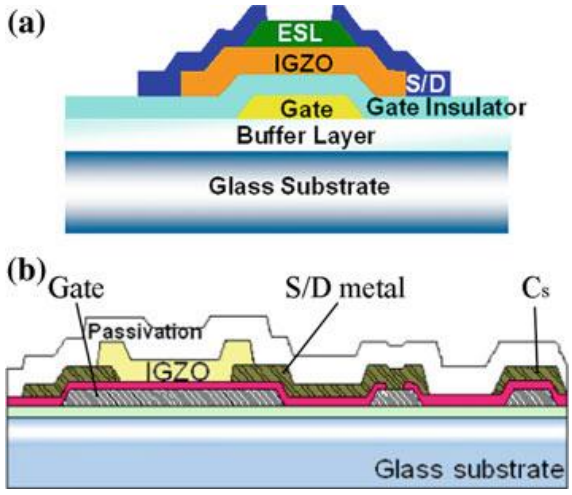


Figure 2.16 a-IGZO TFT structures a) etch-stop and b) inverted coplanar architectures (Osada et al., 2010)

Transfer characteristics of a-IGZO TFT having 200nm thick SiO_x gate dielectric fabricated with PECVD are shown in figure 2.17a. Channel geomerty of this TFT is W=25µm and L=10µm and also, FET mobility, SS slope and on:off ratio ratio values of the TFT are 21 cm^2/Vs, 0.29 V/dec and >10^8, respectively. (Osada et al., 2010). Output characteristics (Kamiya et al., 2009) of another a-IGZO based TFT with a saturation FET mobility value of 11.8 cm^2/Vs are shown in Fig. 2.17.

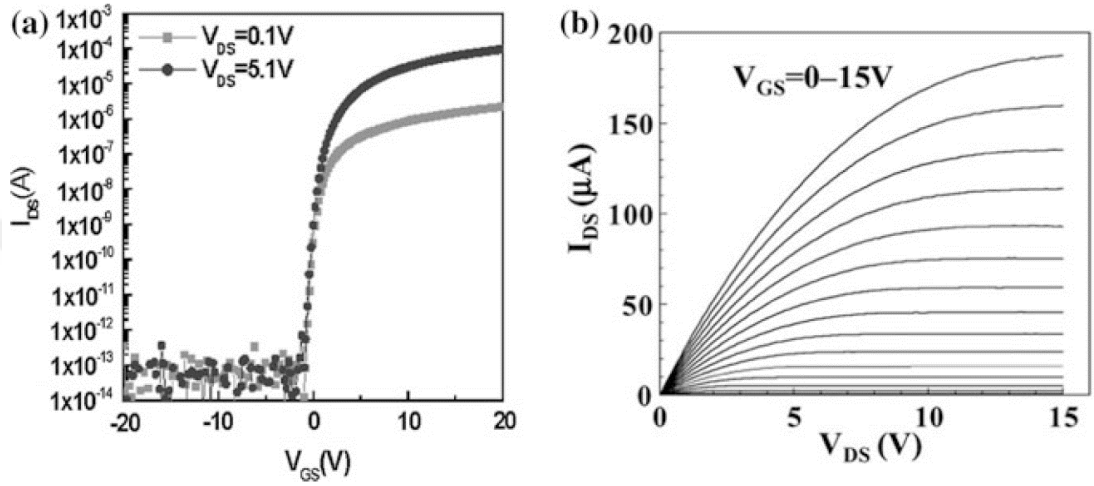


Figure 2.17 ES a-IGZO TFT device a) transfer and b) output characteristics (Kamiya et al., 2009)

2.3 Gate Dielectrics for Oxide TFTs

There have been major advances in the use of oxide semiconductors in TFT structures. However, progress has not been so rapid in dielectric materials that allow charge accumulation at the interface between the semiconductor/dielectric layer.

Si_3N_4 and SiO_2 are used as dieletric layers for a-Si: H TFT (Long et al., 2006; Merticaru et al., 2006) and poly-Si TFT (Dongli & Man, 2006; Mariucci et al., 2004)structures which are a more mature TFT technology, respectively. In addition, the deposition methods (especially PECVD) that will be used to produce these dielectric layers of regarding TFT devices are technologically mature (Carcia et al., 2007; Lim et al., 2008; Wang et al., 2008).

SiO_2 is considered to be the most reliable dielectric material for lots of electronic applications and devices, such as CMOS ICs, due to the fact that it maintains its properties even in the form of natural oxides in interface that it creates with single crystal silicone (Liu et al., 2018; Ozer et al., 2022).

However, when the thickness of the SiO_2 layers approaches the atomic levels, the leakage current density (J_{leak}) values in the respective TFT structures increase due to the direct tunneling effect and power consumption in standby mode of the systems where TFT structures are used reaches large levels that will make serious problems for power consumption of these devices (Liu et al., 2018). But, these technological barriers have been overcome using high dielectric constant materials, such as HfO_2 and other similar oxide materials etc., instead of SiO_2 (Liu et al., 2018; Ozer et al., 2022).

2.3.1 High-K Dielectrics

One of the most important application areas of dielectric materials in electronic devices are thin film transistors (TFTs) (Branquinho et al., 2014; Lee, Jeong, et al., 2017; Lim et al., 2013; Nakano et al., 2012; Park et al., 2009; Rim et al., 2014; Rim et al., 2017). By using different types of dielectric materials in TFT applications, it is possible to develop TFT structures that have different operating voltages and frequencies (Chen et al., 2014; Choi & Song, 2018; Han et al., 2018; Jo et al., 2018; Lee, Shin, et al., 2017; Meena et al., 2011; Ozer et al., 2022; Salvatore et al., 2014).

At the present time, the rapid development of complementary metal oxide semiconductor integrated circuits (CMOS Ics) significantly contribute to development of consumer electronics and microelectronic industries (He et al., 2011; Robertson & Wallace, 2015). SiO_2 is considered to be the most reliable dielectric material for CMOS ICs due to the fact that it maintains its properties even in the form of natural oxides in interface that it creates with single crystal silicone (Liu et al., 2018). In addition to this, nowadays the increasing demands for high performance despite accepted power consumption require a significant reduction in the size per unit area of the related electronic devices , such as field effect transistors (FETs), etc (Liu et al., 2018). This indicates that the FET dimensions within ICs and therefore thickness of the SiO_2 dielectric layers used in these structures also need to be reduced.

Thermally grown SiO_2, which is widely used as a dielectric layer in single crystal silicon technology, probably contributes to the extraordinary properties of metal-oxide-semiconductor field-effect transistors (MOSFETs), thanks to its successful Si/SiO_2 combination. Si/SiO_2 has an almost perfect interface property because thermal SiO_2 is not actually deposited on Si. In addition, it has a gap of about

9 eV and typically over 10 $MVcm^{-1}$ refractive electric field value. These properties have made it a frequently preferred dielectric material for MOSFET applications. (Wallace & Wilk, 2002).

With today's emerging technology, the demand for miniaturization in electronic device architecture requires the thickness of the SiO_2 layer to be less than 1 nm in new generation transistors with channel sizes below 45 nm. This represents a critical problem even for a perfect insulator such as thermal SiO_2, because the gate leakage current increases significantly due to quantum tunneling effects (Hirose et al., 2000). One of the best possibilities to overcome this limitation is the use of high-k dielectrics. In this way, while maintaining the same capacitance per unit area, thicker dielectric films can be used. Research on high-k dielectric materials began in the mid-1990s and now they used in developping of Intel microprocessors architechtures having nano structures below 45 nm. While High k dielectrics allow the required capacitance per unit area and at the sime time they can maintain a physical thickness that can provide low gate leakage current. Thanks to these superior properties, high-K dielectric materials also play an important role in the development of transparent and transparent electronic applications (Hsu et al., 2013; Ko et al., 2011; Mativenga et al., 2015; Mohapatra et al., 2002; Robertson & Wallace, 2015; Wilk et al., 2001).

2.3.2 Requirements

High k dielectrics are of great importance for electronic circuits. However, metal oxide dielectrics with high k value have some disadvantages such as increased parasitic capacitance (Mohapatra et al., 2002) and low band gap (Figure 2.18a) (Barquinha et al., 2012a). Although thicker high k dielectric layers prevent direct tunneling, it provides the same capacitance per unit area for SiO_2. However, if concerning band gap (Eg) value is too low, unwanted gate leakage current may still be a problem (Degraeve et al., 2002). Even if band gap of the dielectric layer is significantly larger than related semiconductor to develop a reliable TFT device the following requirement must also be fulfilled: Offsets of the dielectric valence band maximum (VBM) of a p-type transistor and the dielectric conduction band minimum (CBM) of an n-type transistor should be at least 1 eV relative to that of the semiconductor (Figure 2.18b) (Robertson, 2002).

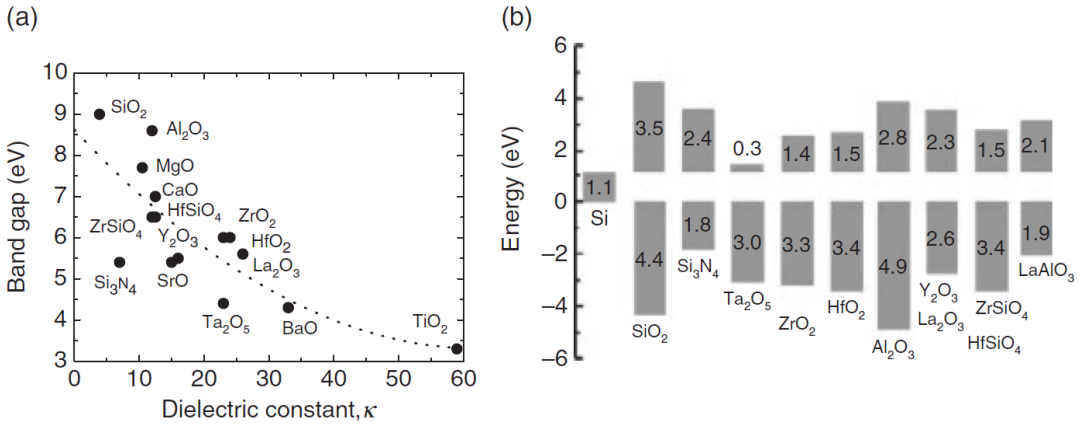


Figure 2.18 a) Band gap energy changing by dielectric constant (Barquinha et al., 2012a) b) band energy for some dielectrics on silicon (Robertson, 2002)

Another important thing to consider is structure of the dielektric materials. Most high-k dielectrics are polycrystalline even when annealed at low temperatures. However grain boundaries in poly-crystalline or crystalline strucutes effect negativily to some electrical properties, such FET mobility, leakage current and etc., of TFT device. On the other hand, amorphous layers allow advantage for this issue do not have grain boundries. Moreover, amorphous materials can provide ultra smooth surfaces even large areas and this helps to improve electrical properties of TFT devices (Robertson, 2002; Wilk et al., 2001). One of the parameters that determine the performance of the transistors is the quality of the dielectric/semiconductor interface. Most high-k dielectric materials have mid-gap interface state densities (Wilk et al., 2001). Another important point for the selection of high-k dielectric material is that the related dilelectric material is thermodynamically stable with the semiconductor and should be suitable for the relevant TFT production method (Wilk et al., 2001).

The consideration regarding band gap is even more important in oxides TFTs. In Figure 2.19, it is shown the results of a study for ZnO semiconductor and high-k dielectric materials (King et al., 2009; Lin et al., 2002; Robertson et al., 2006). The information described here, the basic properties of some high-k dielectric materials are given in Table 2.3.

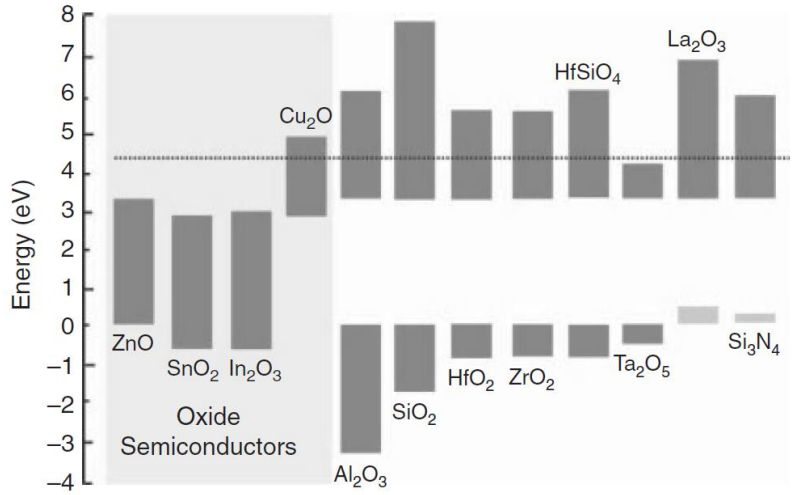


Figure 2.19 Band offset energy for some dielectrics (Barquinha et al., 2012a)

Table 2.3 Important parameters of some dielectrics (Barquinha et al., 2012a)

Dielectric	**κ**	**E_g (eV)**	**ZnO CBO (eV)**	**SnO_2 CBO (eV)**	**In_2O_3 CBO (eV)**
SiO_2	3.9	9.0	4.3	4.8	4.6
Al_2O_3	9	8.8	3.6	3.1	2.9
Si_3N_4	7	5.4	2.5	3.0	2.8
HfO_2	25	6.0	2.1	2.6	2.4
La_2O_3	30	5.7	3.4	3.9	3.7
Ta_2O_5	26	4.4	0.9	1.4	1.2
ZrO_2	24	5.8	2.0	2.5	2.3
$HfSiO_4$	14	6.5	2.7	3.2	3.0

2.3.3 Deposition of High-K Dielectric Materials for TFTs

Solution and gas phase processes are most common method to produce high-κ dielectric materials. CVD and PVD methods are frequently used for gas phase process at fabrication of high-κ dielectrics. For solution-based processes, the sol-gel method is widely used to deposit dielectric thin films. Some advantages of this method include high purity production, ease of composition control, and the possibility of large area deposition. However, to obtain dried layer deposition on the related substare, it needs

annealing of the concerning material around 400 ºC (Lin et al., 2002). One of the disadvantages of this method is that it can cause crack formation on related surface.

For CVD method, atomic layer deposition (ALD) (Cho et al., 2002; Lin et al., 2002) and metalorganic chemical vapour deposition (MOCVD) (Cheng et al., 2004; Frohlich et al., 2006) methods widely prefer to producu dielectric layer. Due to the fact that growth process with these methods can control layer by layer, these techniques provide good stochiometry, nice coverage of whole surface and good insulating characteristics. Although the MOCVD method has a great potential, it is a major problem that the relevant layer needs to be heated up to around 350 °C in order to remove organic compounds from the related layer (Abermann et al., 2007; Lehn et al., 2006; Ohshita et al., 2006). High purity fabrication is the most advantage of ALD method. However, it is disadvantages of this metod that has too low deposition rate and needs temperature above 250°C during deposition process (Carcia et al., 2006; Jones et al., 2004).

Some of the physical vapor deposition (PVD) techniques that can be used to precisely deposit high-κ dielectrics on the surface of interest are sputtering, PLD, and thermal evaporation method (Atanassova & Paskaleva, 2002; Callegari et al., 2001; Chowdhury et al., 2004; Honda et al., 2004; Lebedinskii et al., 2005; Xing et al., 2003). The sputtering method is widely used for dielectric material deposition on a surface due to its advantages, such as easily controllable growth steps, allowing large-scale applications, and low-temperature processing. Since it enables TFT production especially at low temperatures, it is of great interest in the production of flexible devices on low cost polymer substrates. As an example, deposition of several high-k oxides such as HfO_2 (Kirsch et al., 2002; Pereira et al., 2004; Tsui & Chang, 2003), Ta_2O_5 (Chaneliere et al., 1998; Grüger et al., 2004), ZrO_2 (Chim et al., 2003; Qi et al., 2000), La_2O_3 , Y_2O_3 (Evangelou et al., 2003; Pan & Lee, 2007) can be made by sputtering method. Some electrical properties of TFT structures using high-k dielectric materials are shown in table 2.4 (Barquinha et al., 2012a).

Table 2.4 Important electrical parameters of some oxide TFTs having high-k dielectric layer (Barquinha et al., 2012a)

High- κ	Semic.	Dielectric Thickness (nm)	μ (cm^2/Vs)	SS (V/dec)	V_T (V)	I_G (A)
HfO_2	GIZO	-	7.2	0.25	0.44	-
HfO_2	ZnO	250	1	-	-	$<10^{-9}$@4V
HfO_2	GIZO	180	8.4	0.25	-1	-
HfO_2	ZnO	200	14.7	-	2	-
Y_2O_3	GIZO	140	12	0.2	1.4	-
Ta_2O_5	GIZO	200	61.5	0.61	0.25	-
Ta_2O_5/SiO_2	GIZO	300	35	0.24	-	-
ZrO_2	GIZO	200	28	0.56	3.2	$<10^{-8}$@10V

2.3.4 Multilayer Dielectrics

High-k dielectric materials should be used in these devices in order to reduce the operating voltage of oxide TFTs. This can not allow possible by using SiO_2 as gate dielectric material. However, due to its wide band gap, SiO_2 is still of interest as a gate dielectric material and the κ value drop can be minimized by using a multi-layer gate dielectric structure with appropriate SiO_2 thickness (Barquinha et al., 2012a).

$SiO_2/HfO_2/SiO_2$ (S–H–S) structures with a thickness of around 20/180/20nm is good example for multilayer dielectrics. The XRD data shows related peaks for lattice structure of S-H-S (Figure 2.20). There are crystalline structure in between two amorphous interface layers. According to AFM results, RMS roughness of multilayer structure is much lower than in single HfO_2. According to these results, top SiO_2 layer works as a buffer to obtain smoother surfaces. When biased under the sputtering process, it is seen that orthorhombic phase of HfO_2 begins to form predominantly. However, again there is no crystal structure formation for SiO_2. In addition to this, the surface roughness in these stacks can be adjusted under bias during sputtering process (Fig. 2.21). Here, the change in RMS value is related to the damage of the surface of SiO_2 caused by ionic bombardment of the relevant substrate during the sputtering process. Here, the change in RMS value is related to the damage of the surface of SiO_2

caused by ionic bombardment of the relevant substrate when it is applied bias to substrate during the sputtering process (Barquinha et al., 2012a).

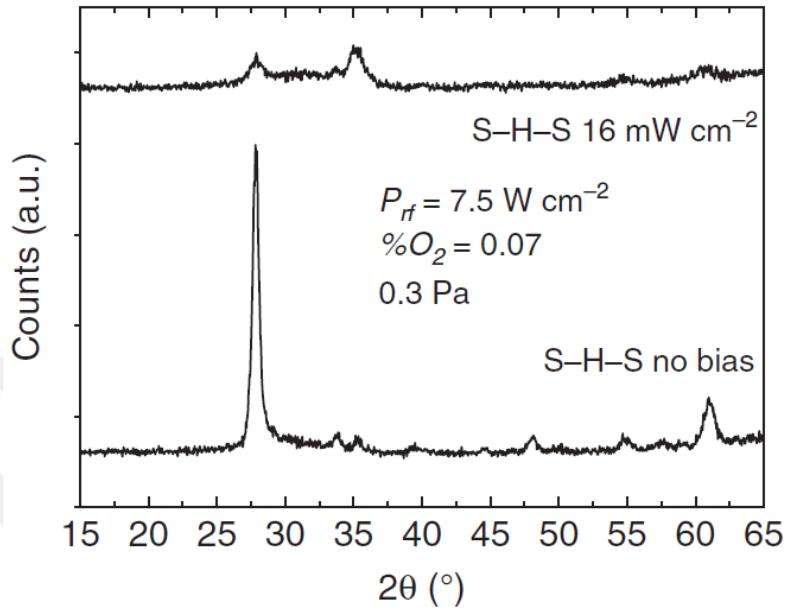


Figure 2.20 XRD data of S-H-S multilayer thin film structure (Barquinha et al., 2012a)

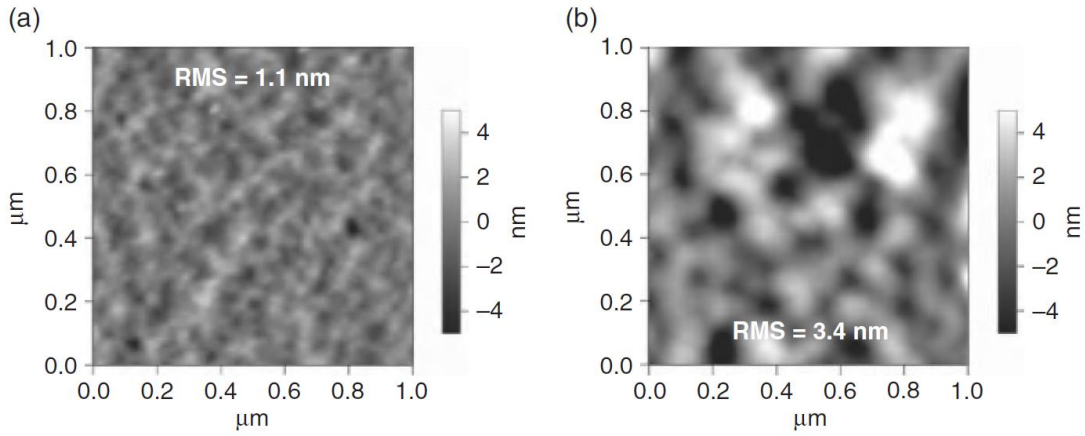


Figure 2.21 AFM image of S–H–S multilayer multilayer thin film a) without bias for substrate and b) with bias (Barquinha et al., 2012a)

Another option is to use HSiO films instead of HfO_2 between SiO_2 layers. This structure is called S - HS - S. The multilayer film, which also occurs in this structure, is amorphous because all the layers used in the structure can be produced as

amorphous. In addition, the surface roughness value of the structure is below 1 nm (Figure 2.22) (Barquinha et al., 2012a).

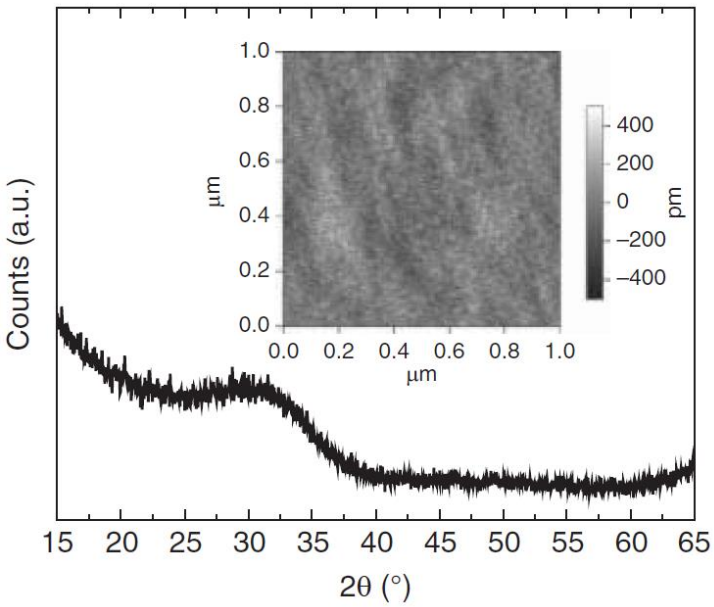


Figure 2.22 XRD pattern and AFM image of a S–HS–S multilayer thin film structure (Barquinha et al., 2012a)

As a different approach, metal insulator semiconductor structures in c-Si were used that is shown in Figure 2.23 to control the insulating ability of these multilayer structures. The new structure in here is the S-H-S-H-S and this new and previous structure has been compared for bias and unbias conditions. In the wihout bias condition, when the number of layers increases, leakage current of TFT device decreases and also breakdown voltage increases from 2 to about 4 $MVcm^{-1}$. This is because electrons have to travel through a longer dielectric layer. However, combaning multilayer dielectric with the substrate biasing is a much more effective method. Surface damge can be minimized by adjusting P_{bias} value and the current density can be imporved via the same parameter at the same time. Breakdown voltage for concerning films used in this study is above 5 $MVcm^{-1}$. Also, dielectric constant of this multilayer structure decreases from only 14 to 9.5 for the S-H-S and S-HS-S, respectively (Barquinha et al., 2012a).

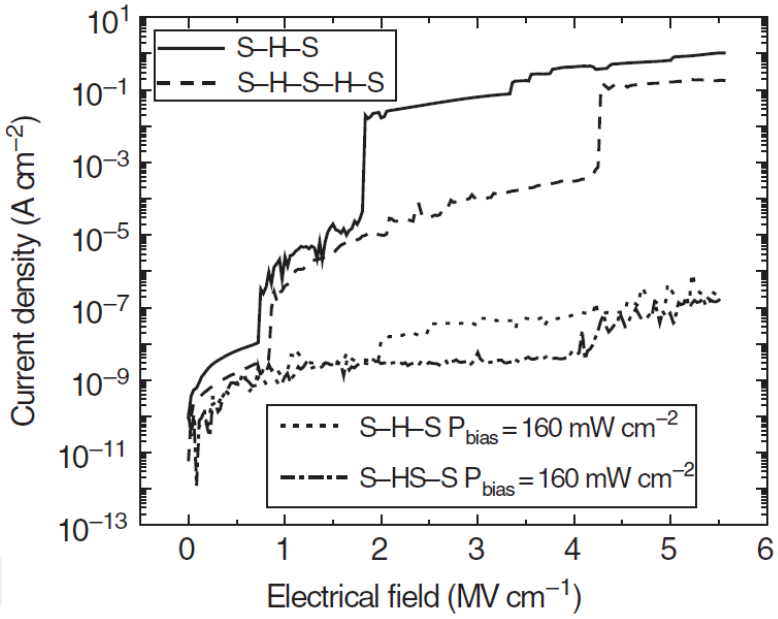


Figure 2.23 Electrical field vs. current density characteristics of MIS structures with or without substrate bias configurations (Barquinha et al., 2012a)

In summary, multilayer dielectric structures can be considered good insulation layers for oxide TFTs. If the SiO_2 thickness can be preciesly adjusted to prevent direct tunneling effect, these structures can act as an effective barrier to inhibit electron trapping at the interfaces between dielectric and semiconductor layers on TFTs. Polycrystalline or amorphous HfO_2-based layers can be used between two interfacial SiO_2 layers. Thus, the final surface morphology of these stack layers depends on the structure and bias conditions of the substrate on which they are grown. However, a multilayer gate dielectric with each layer produced amorphous is promising for oxide TFTs. Because the structures produced in this way can greatly reduce the leakage current value of the oxide TFT (Barquinha et al., 2012a).

2.3.5 High-K Dielectrics / Oxide Semiconductor Interface

In the light of these studies in the literature, it is clearly seen that when materials with high dielectric constant such as $Al2O_3$, ZrO_2 and HfO_2 compared to materials with low dielectric constant such as SiO_2 are used as a gate insulating layer in TFT structures, the electrical properties and operating performances of the relevant TFT device increase (Chen et al., 2014; Salvatore et al., 2014).

But, the dielectric constant of the relevant material is not the only parameter to be taken as a basis in the selection of the gate insulating layer for TFT structures. In these structures, it is known that the region where electrons move mainly is the interface formed between the gate insulating layer and the semiconductor layer. In this context, the effect of the interface between the semiconductor material used in TFT structures and the relevant insulating layer on the electron mobility should be well known.

One of the most popular semiconductors used in oxide TFT structures in literature is IGZO. In one of the studies in the literature, it has been shown that electrons can be trapped around weak metal-oxygen bonds in the oxide lattice at the interface between the IGZO-based semiconductor layer and the SiO_2-based dielectric layer (Kang et al., 2017; Ozer et al., 2022). The electronegativity of the bond at the interface of SiO_2 and IGZO directly affects this situation. Si atoms have less ability to bond with O atoms than In, Ga and Zn atoms. Because Si atoms have higher electronegativity compared to these atoms. In this case, electrons moving within the relevant interface can be trapped in this region.

In this TFT structure, the electrical performance of the relevant TFT structure could be increased by modifying the SiO_2 surface with a material with high dielectric constant such as TaOx. With the new modification in TFT structure, it forms a new interface between the IGZO semiconductor and TaOx. Since the ability of Ta atoms to bond with O atoms is higher than that of In, Ga and Zn atoms, the number of oxygen spaces in the newly formed oxide lattice structure in the interface has decreased considerably compared to the interface with SiO_2. The XPS results in Figure 2.24 clearly confirm this situation.

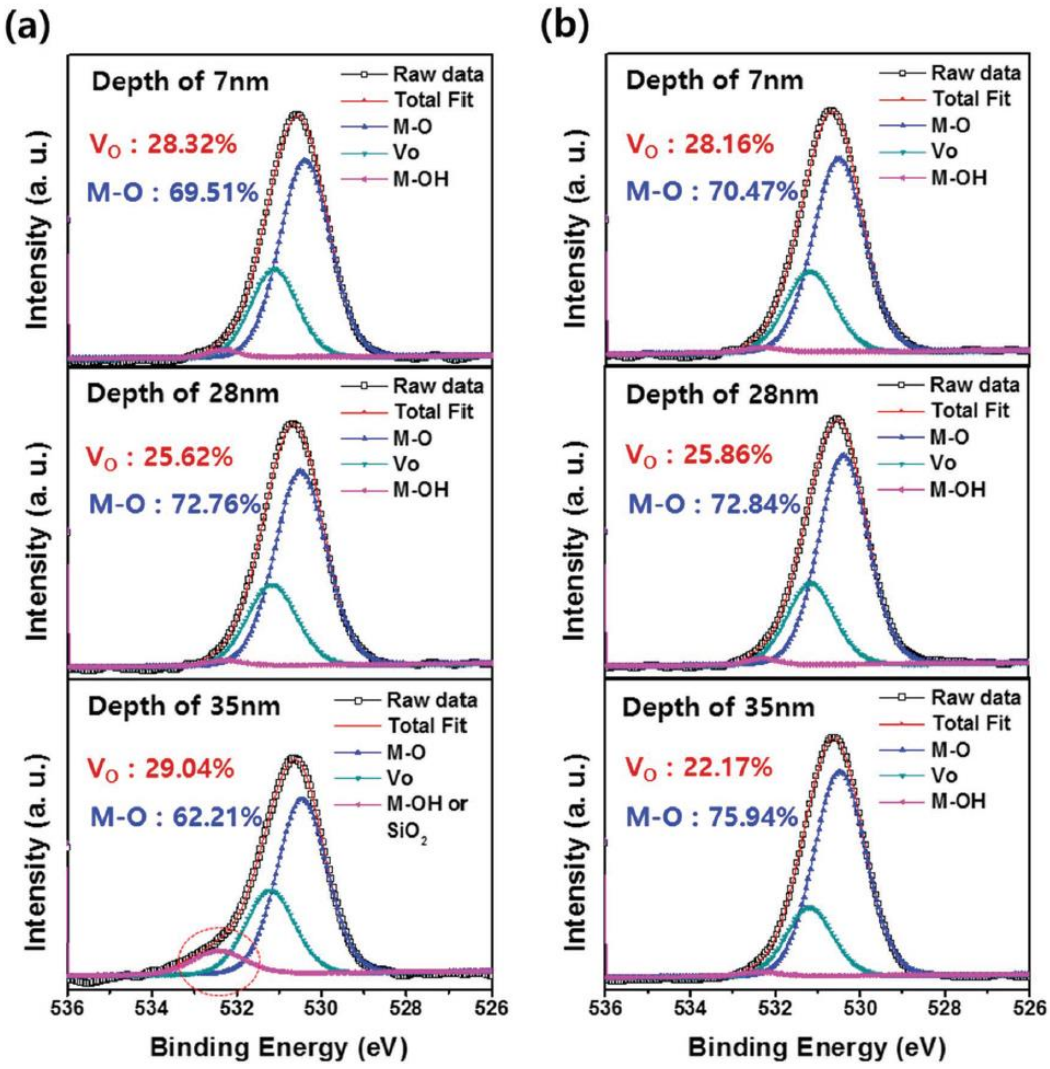


Figure 2.24 O1s XPS depth analysis results from 7, 28, and 35 nm depths a) without TaOx modification and b) with TaOx modification (Kang et al., 2017)

The reduction of oxygen spaces in this new structure reduced the possibility of trapping electrons, and this situation provided a significant increase in the electrical performance of the TFT structure. When the FET mobility, Vth and SS values of the newly developed TFT structure are examined, it is clearly seen that the electrical properties of this structure increase (See Table 2.5).

Table 2.5 Detailed electrical parameters of interface imporved TFT without TaOx (sample A) and with (sample B) 6nm TaOx interface modification (Kang et al., 2017)

Type of Sample	**μ_{sat} ($cm^2V^{-1}s^{-1}$)**	**V_{th} (V)**	**SS ($V\ dec^{-1}$)**	**$I_{on/off}$**
Sample A	12.78 ± 1.03	-0.32 ± 0.42	0.57 ± 0.07	$\approx 10^7$
Sample C	19.14 ± 2.41	-1.12 ± 0.18	0.23 ± 0.02	$\approx 10^8$

With a similar approach, this time, the surface of the SiO_2 dielectric layer was modified with $Y_2O_3/TiO_2/Y_2O_3$ triple dielectric layer structure, and improvements were achieved in the electrical properties of the IGZO semiconductor based TFT structure (Hsu et al., 2013). Here, it is seen that important electrical parameters such as V_{OP}, V_{Th}, μ_{FET}, SS and I_{on}/I_{off} ratio are improved (See Table 2.6) when compared to their counterparts in the TFT structure in which the dielectric layer in the newly developed YTY structure is used.

Table 2.6 Low temperature annealed IGZO TFTs on different substrates (Hsu et al., 2013)

High- κ	**V_{OP} (V)**	**V_T (V)**	**μ (cm^2/Vs)**	**SS (mV/dec)**	**V_T (V)**	**Process**
YTY	3	0175	32.7	137	2.4×10^5	RT/PC
SiO_x	5	-1.35	18	100	1×10^5	RT/PI
SiN_x	10	1.13	5.3	550	8×10^4	<100 °C/PI
SiO_x	10	1.9	1.2	650	1×10^4	100 °C/Paper
SiN_x	6	1.25	12.1	350	$>10^5$	90 °C/PET
Y_2O_3	6	1.4	3.9	200	1.7×10^6	RT/PET
BST-MgO	15	4.2	1.04	1850	7.48×10^5	RT/PET
ZrO_2	10	3.2	28	560	$>10^7$	RT/Glass
Ta_2O_5:SiO_2	15	0	35	240	3.3×10^6	150 °C/Glass

2.4 Semiconductor Layers for Oxide TFTs

There are many different semiconductor options for oxide TFTs such as p-type and n-type (Shin et al., 2009). Some of the polular oxide semiconductors are SnO, CuO and IGZO (Gutierrez-Heredia et al., 2017; Mativenga et al., 2015; Ogo et al., 2008; Park et al., 2012; Xiao et al., 2018).In addition to their high mobility, oxide semiconductors are of great importance in display applications, which are one of the widely used areas of TFT technologies, with their long-term stable operation performance (Gutierrez-Heredia et al., 2017; Park et al., 2012; Xiao et al., 2018). IGZO semiconductor material attracts great attention with the developing technology in this field.

The fact that IGZO can be produced as amorphous, has a high mobility value even in amorphous structure and maintains its stability in the long term, makes it possible to use TFTs consisting of a semiconductor layer a-IGZO in large area display applications (Park et al., 2012). Figure 2.25 shows the electrical performance of a TFT with a semiconductor layer a-IGZO.

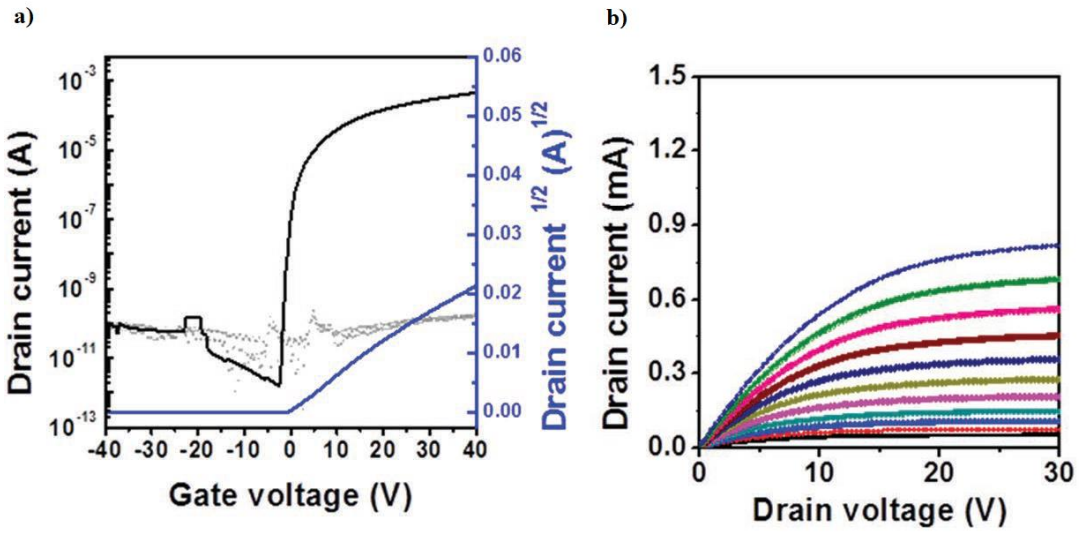


Figure 2.25 Electrical characteristics for a-IGZO TFT a) transfer and b) output characteristics (Kang et al., 2017)

The biggest difference of a-IGZO from other oxide semiconductors is that its optical transmittance value is over 70% for the visible region (Mativenga et al., 2015). This feature made it possible to use a-IGZO in the production of both flexible and

transparent TFT structure (Gutierrez-Heredia et al., 2017; Mativenga et al., 2015; Xiao et al., 2018). Optical transmittance spectrum of a-IGZO based TFT is shown in Figure 2.26 and electrical properties of the same TFT structure are shown in table 2.7.

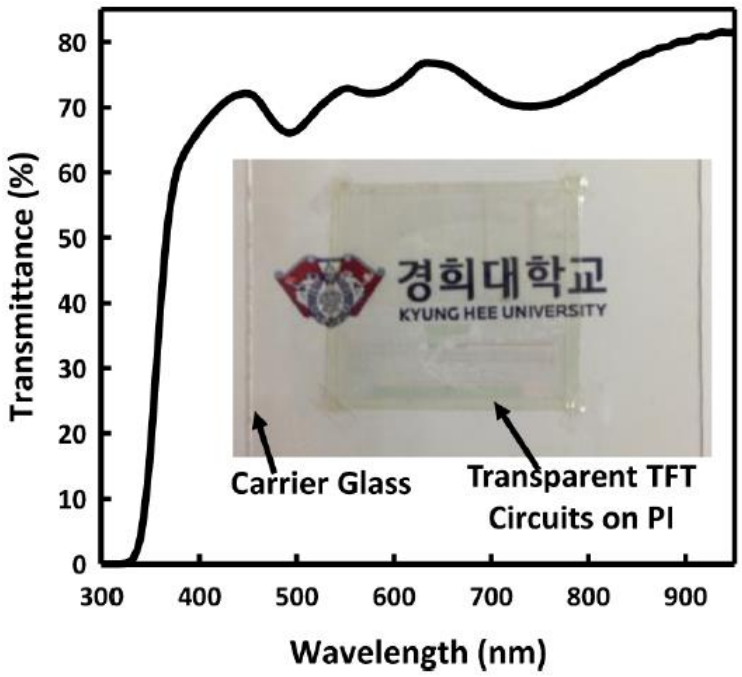


Figure 2.26 Optical transmission spectrum of a-IGZO TFT (Mativenga et al., 2015)

Table 2.7 Electrical properties of a-IGZO based transparent flexible TFT (Mativenga et al., 2015)

	Before detachment (on glass / CPI)		**After detachmant (on CPI)**	
	Mean	Standart deviation	Mean	Standart deviation
μ (cm^2/Vs)	12.50	0.34	12.70	0.46
V_{ON} (V)	-1.50	0.33	-1.74	0.17
SS (mV/dec)	156	14	160	29

The fact that IGZO can be produced as amorphous, it has enabled to have a superior performance mechanically. Figure 2.27 shows the change in the electrical performance of the TFT structure, which has been mechanically stretched many times, during the process. As it can be seen here, due to the fact that the a-IGZO structure does not have

grain boundaries allows the related TFT to maintain its electrical performance even if it is subjected to mechanical stretching many times in the long term (Mativenga et al., 2015).

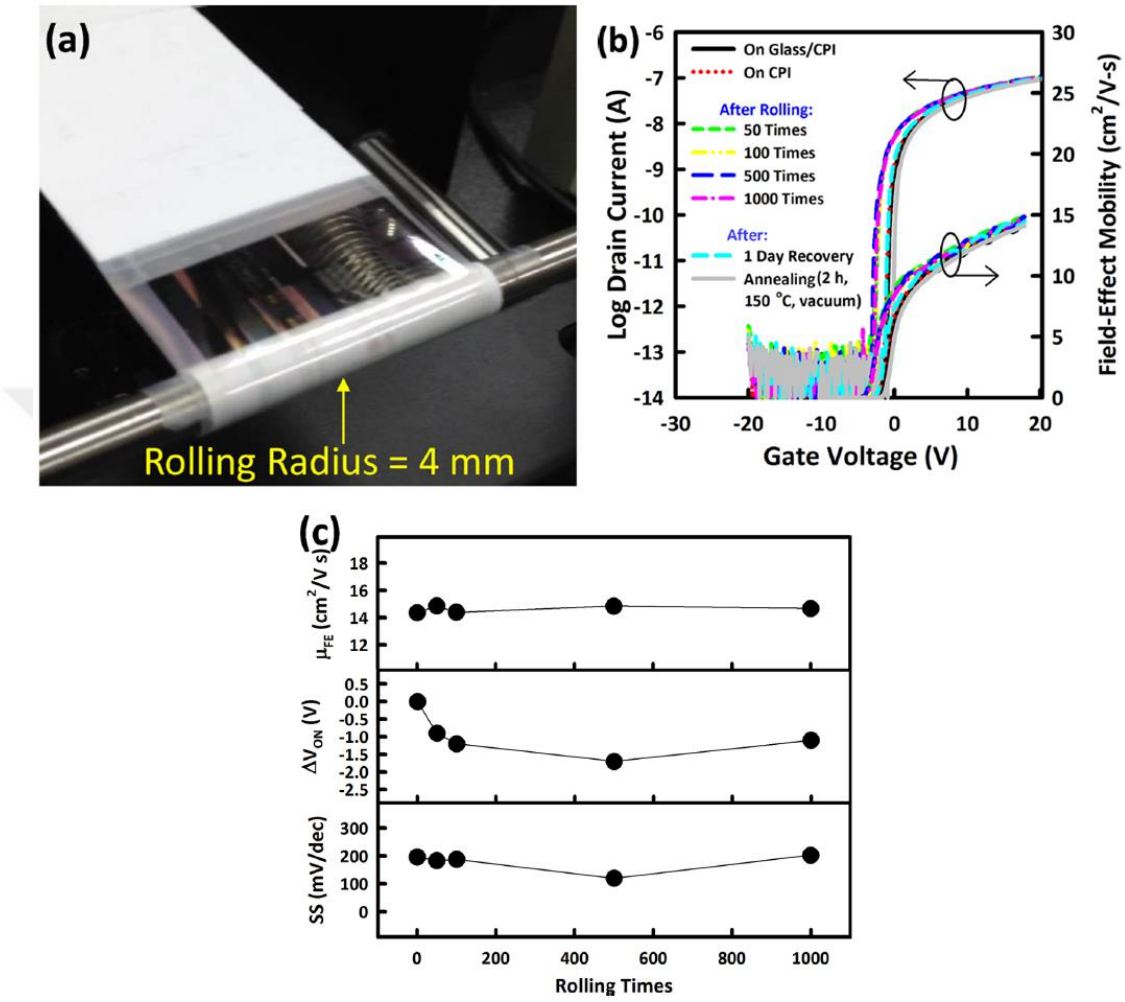


Figure 2.27 Changing of electrical characteristics and parameters of fully transparent rollable a-IGZO TFTs after some rolling cycle (Mativenga et al., 2015)

2.5 Flexible and Transparent TFTs

A transparent, flexible and unbreakable display can also be worn or used for advertising purposes in automobiles (Branquinho et al., 2014; Lee, Jeong, et al., 2017; Lim et al., 2013; Mativenga et al., 2015; Nakano et al., 2012; Park et al., 2009; Rim et al., 2014). However, today there are many different flexible transparent display applications.

One of the most popular research areas for transparent and flexible display technologies is flexible and transparent TFTs. Various flexible and transparent substrates are used for these device structures (Knobelspies et al., 2016; Münzenrieder et al., 2015; Park et al., 2012; Rembert et al., 2015; Xiao et al., 2018). However, the most popular subjects that are studied to make this structure transparent are on the semiconductor layer of the TFT structure. In these studies, AOSs are among the prominent semiconductors (Gutierrez-Heredia et al., 2017; Mativenga et al., 2015; Park et al., 2012; Xiao et al., 2018). Popular AOS such as IGZO show very high optical transmittance in the visible region of the electromagnetic spectrum (Knobelspies et al., 2016; Mativenga et al., 2015; Rembert et al., 2015). For this reason, IGZO is one of the most suitable AOSs that will can be used in flexible transparent TFT structures for display applications.

2.5.1 Architechture of Flexible and Transparent TFT Devices

In order to make a TFT structure flexible, the substrate used in its production must also consist of a flexible material. The most preferred substrates for such a TFT structures are polymer materials (Gutierrez-Heredia et al., 2017; Mativenga et al., 2015; Münzenrieder et al., 2015; Xiao et al., 2018). PEN, polyamide, and parylene can be given as an example to polymer substrates (Gutierrez-Heredia et al., 2017; Mativenga et al., 2015; Xiao et al., 2018). Another important feature of these polymer-based materials should be transparent (Rembert et al., 2015). The architectures and electrical properties of some transparent TFTs are shown in Figures 2.28, 2.29 and 2.30.

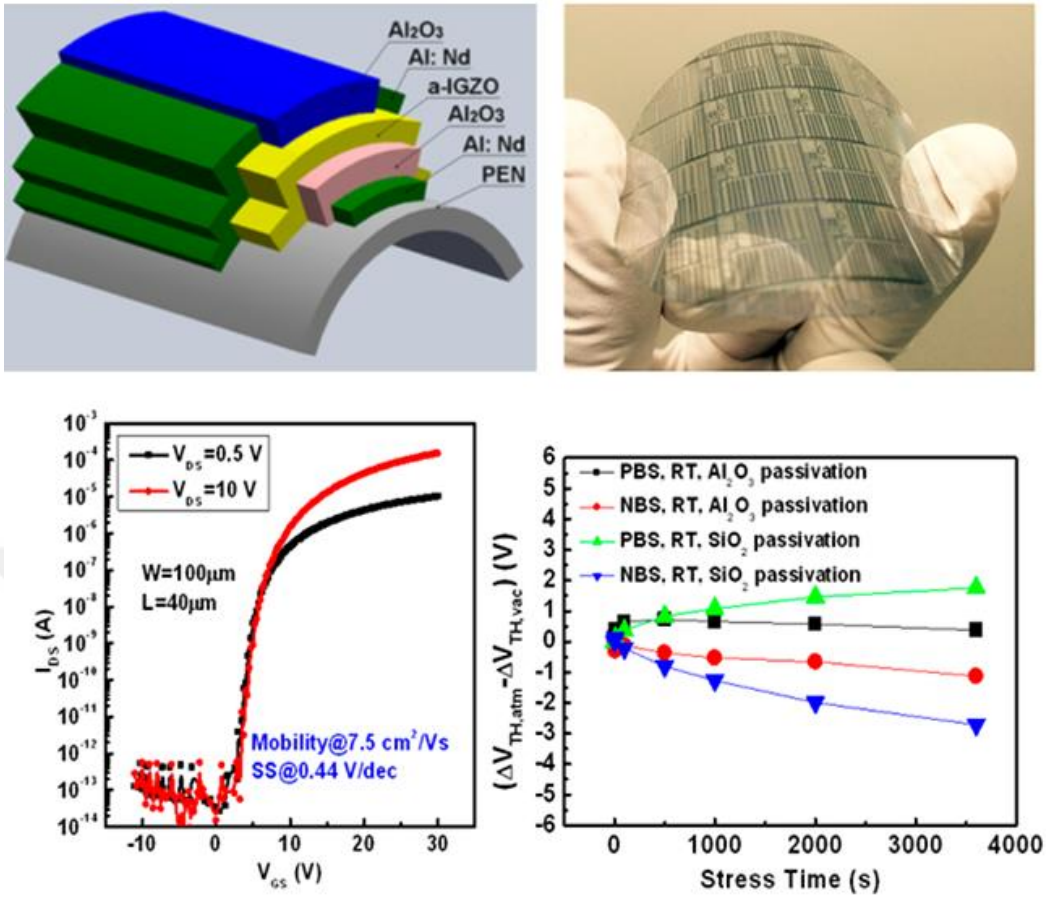


Figure 2.28 Electrical characteristics of flexible a-IGZO TFT fabricated the room-temperature (Xiao et al., 2018)

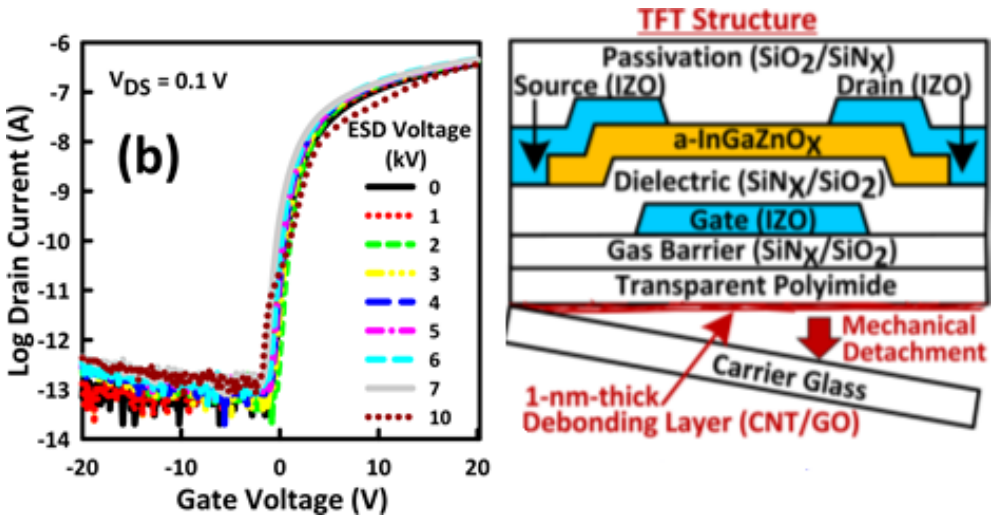


Figure 2.29 Electrical characteristics a transparent TFT based on of a-IGZO semiconductor (Mativenga et al., 2015)

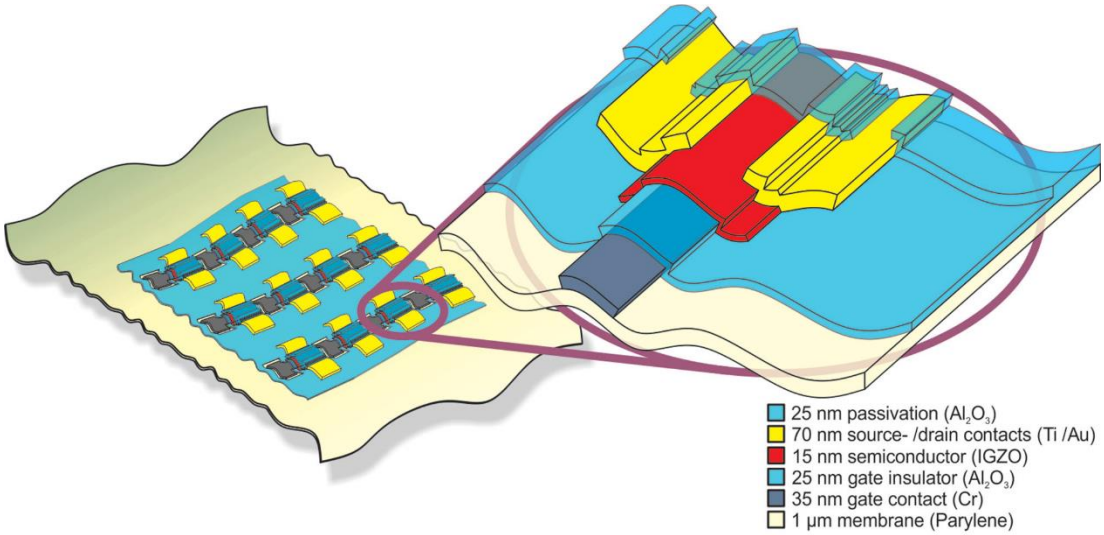


Figure 2.30 Structure, materials, and layer thicknesses of the a-IGZO based flexible oxide TFTs (Münzenrieder et al., 2015)

One of the important features of some of the popular AOS such as IGZO is that they can be produced transparently. However, it is not enough to produce the semiconductor layer and other layers in the TFT structure as transparent to make the whole structure transparent. In order to make a TFT structure completely transparent, its contacts in the relevant TFT structure must be transparent (Liu et al., 2014; Rembert et al., 2015). Frequently preferred contact materials in transparent TFT structure are TCO materials such as ITO, IZO (Liu et al., 2014; Rembert et al., 2015). The architectures and electrical properties of flexible transparent TFTs are shared in Figures 2.31 and 2.32.

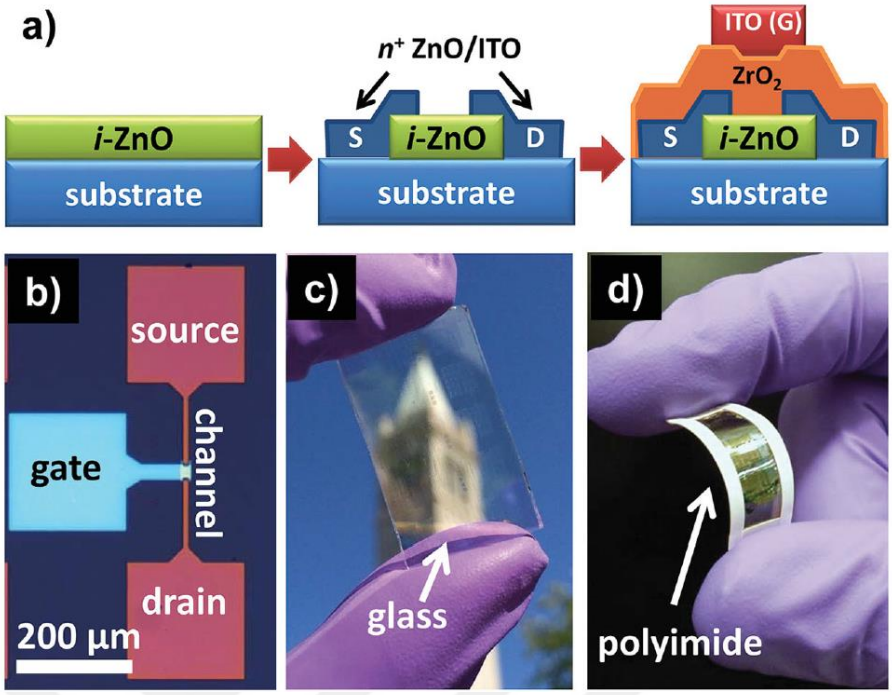


Figure 2.31 Transparent and flexible ZnO based TFT (Rembert et al., 2015)

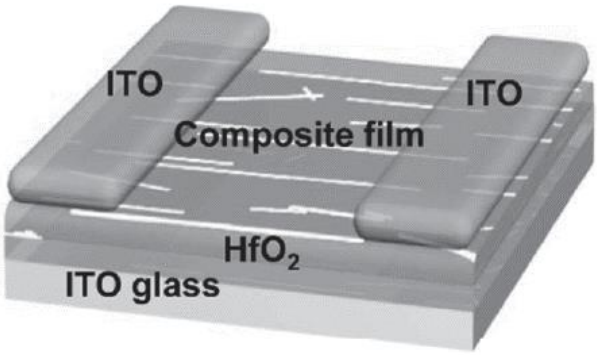


Figure 2.32 Schematic of a-IGZO based transparent TFT device (Liu et al., 2014)

2.5.3 Applications Areas of Flexible and Transparent Electronics

Recently, OLED and LCD panels using a-IGZO-TFT as a backplane were presented at the SID Annual Meeting and SID display meetings. LG electronics presented 4 inch AM full-color OLED display using this backplane option in SID'07 (Kim, 2012). This is the first demonstration that oxide semiconductor TFTs are used as a backplane on OLED displays. Subsequently, a flexible OLED application has presented in IMID'07 by placing a-IGZO on a thin stainless plate (Hayashi et al., 2012). Figure 2.33 shows an developed flexible a-IGZO TFT array and a photograph of the OLED display using this TFT structure as a backplane. SID'07 was a milestone for TAOS-TFTs because, as a technical session on oxide TFT has launched for the first time at the largest and most important conference in the field of display. In SID'08, these TFT structures were brought to the fore as the backplane of LCD and OLED screens. Samsung SDI showed a 12.1" WXGA AMOLED prototype display with a-IGZO TFT backplane that shown in Figure 2.34 (Jeong et al., 2008).

Samsung has been able to successfully generate the a-IGZO TFT array using the same lithographic processes as the a-Si:H TFTs. TAOS-TFTs are now more interesting as the backplane of new generation liquid crystal displays (LCDs). Larger size and higher frame frequency have become a necessity today for the new generation LCDs. When the screen size is increased to > 60 inches, the number of TFTs required has to increase to maintain the same pixel density at the current size. In such a case, the "open" resistance of the TFT arrays can reach levels that cannot be neglected. However, the doubling of the frame frequency (60–120 Hz) is rapidly spreading today. Therefore, the performance of a-Si:H TFTs is insufficient to meet these requirements as shown in Figure 2.35. This is one of the reasons why the researches of a-IGZO TFTs in LCD applications speed up. Samsung Electronics and SAIT presented a 15 inch AM-LCD panel with a-IGZO backplane (Lee et al., 2012).

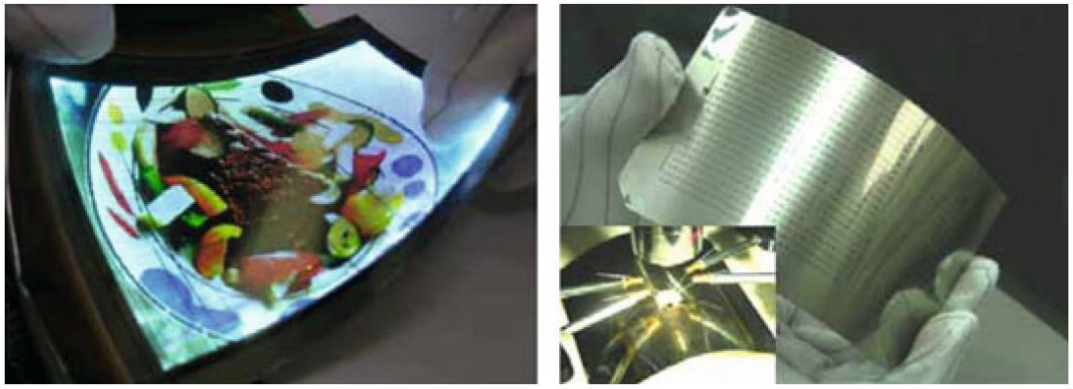


Figure 2.33 4 in. AM-OLED display using flexible a-IGZO TFTs in backplane side (Kim, 2012)



Figure 2.34 2 in. AM-OLED panel with ES structure TFT as backplain options (Hayashi et al., 2012)

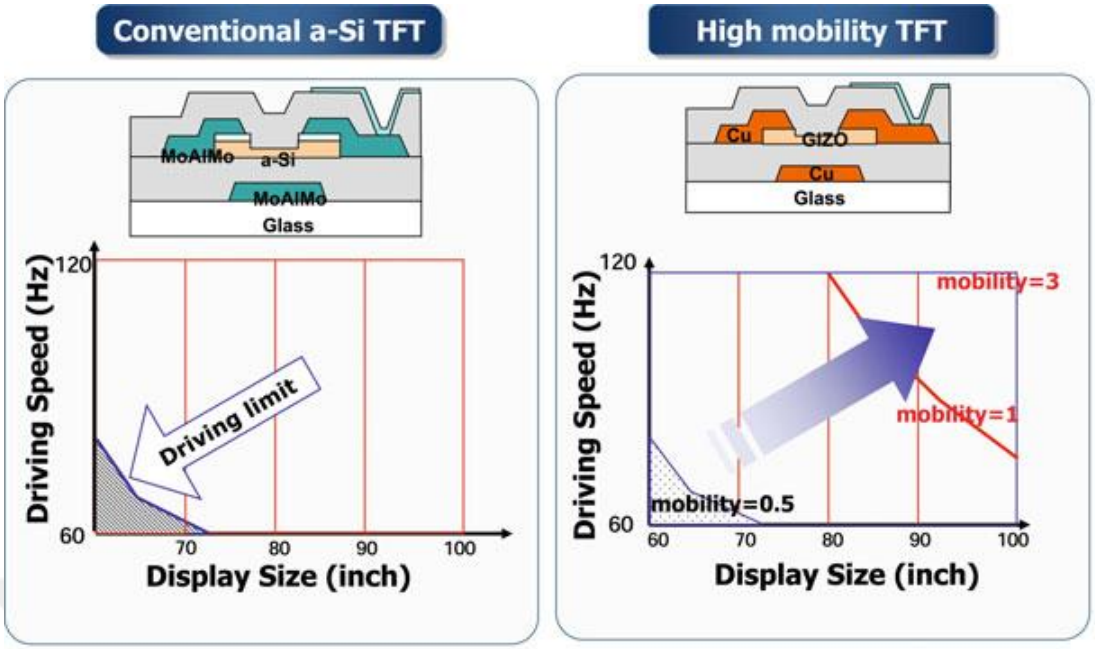


Figure 2.35 Driving speed requirement with display size (Ginley et al., 2010)

In addition, transparent and flexible OLED applications (Hsieh et al., 2010; Nakano et al., 2012) (See Fig. 2.36) and transparent micro-LED display applications (Fan et al., 2019) (See Fig. 2.367 using AOS TFT as backplane option are among the research topics that attract attention in the literature.

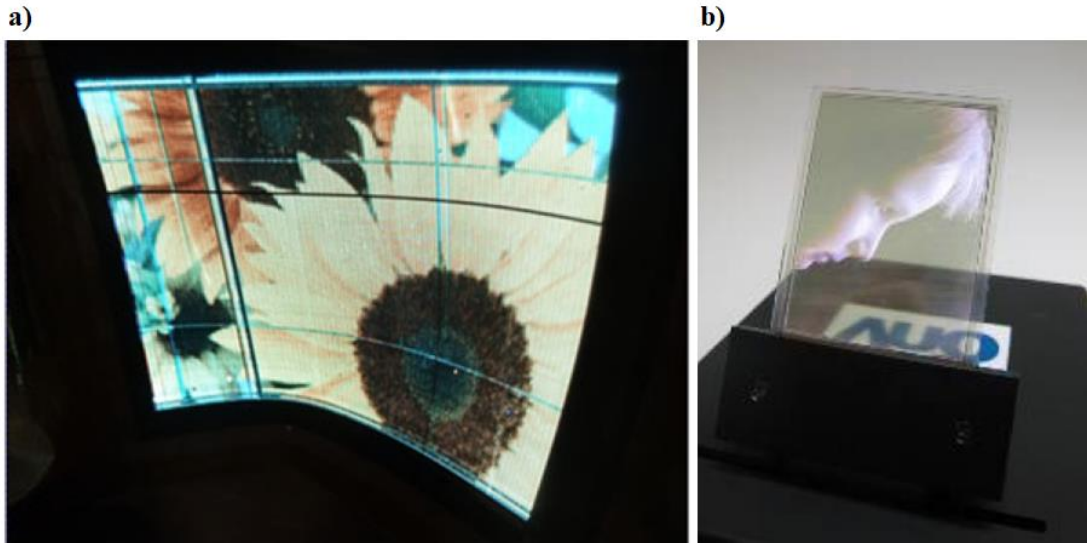


Figure 2.36 OLED applications a) 3" flexible AMOLED display (Nakano et al., 2012) and b) 2.4" transparent AMOLED dispaly (Hsieh et al., 2010)



Figure 2.37 8” transparent micro-LED display (Fan et al., 2019)

CHAPTER THREE

EXPERIMENTAL PROCEDURE

3.1 Purpose

The aim of this study is to develop a long-term stable, flexible and transparent TFT structure that can bring innovative aspects to display technologies. In this context, a-IGZO based TFT structure is produced on flexible PET substrate. Elemental, structural, optical and morphological analyzes were performed for the relevant layers of the fabricated TFT. At the end of this study, long-term stability tests and electrical characterization of this flexible transparent TFT that developed were carried out.

3.2 Materials

Flexible transparent TFT production has been carried out using the sputtering method in order to be suitable for large area applications. For gate dielectric layer, buffer layer, semiconductor layer and Source-Drain contacts of related TFT structure, it was used HfO_2, $SrTiO_3$, IGZO and ITO sputtering targets, respectively. In addition to this, ITO coated PET film was used for flexible and transparent substrate of TFT. All concerning layers was fabricated on this substrate. Target materials was supplied from “Kurt J. Lesker” company and related substrate was supplied form “Sigma Aldrich” company. Detailed information about substrate and target materials used in flexible transparent TFT production are shown in Table 3.1 and Table 3.2, respectively.

Table 3.1 Information of ITO coated PET sheet

Material	Substrate Dimension	Surface Resistivity	Coated Layer Thickness
ITO Coated PET	1 ft × 1 ft × 7 mil	60Ω/sq	100nm

ITO coated PET sheet that was supplied from "Sigma Aldrcih" company was divided into 20mmx15mm pieces for TFT production.

Table 3.2 Material information for sputtering process

TFT Layers	Material	Desnsity (g/cm^3)	Z-Ratio	Purity	Target Diamter (inch)
Gate Dielectric Layer	HfO_2	9.68	1.00	%99.95	2
Buffer Layer	$SrTiO_3$	4.81	0.31	%99.90	2
Semiconductor Layer	IGZO	6.12	1.00	%99.99	2
Source-Drain Contacts	ITO	7.14	1.00	%99.99	2

E322 and E312 model shadow mask and evaporation stack provided from "Ossila" company were used to create the Souce-Drain contacts of TFT. Details on these products are shown in tables 3.3 and 3.4 and in figures 3.1 and 3.2.

Table 3.3 Detailed information for E322 shadow mask

Mask Dimensions	Number of TFTs on One Substrate	Channel Width	Channel Length
20mm x 15mm	20	1mm	30, 40, 50, 60, 80 µm (4 of each)

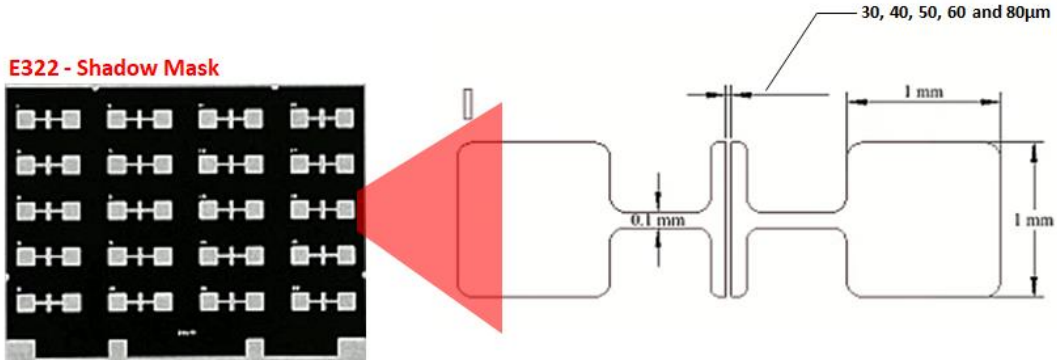


Figure 3.1 Pad dimensions for E322 shadow mask

Table 3.4 Detailed information for E312 evaporation stack

Size	Thickness	Material	Substrate capacity
75mm x 75mm	2mm	▪ Lower support: milled aluminium ▪ Lid: stainless steel ▪ Magnetic sheet: vinyl-laminated polymer resin with ferrite powder	12

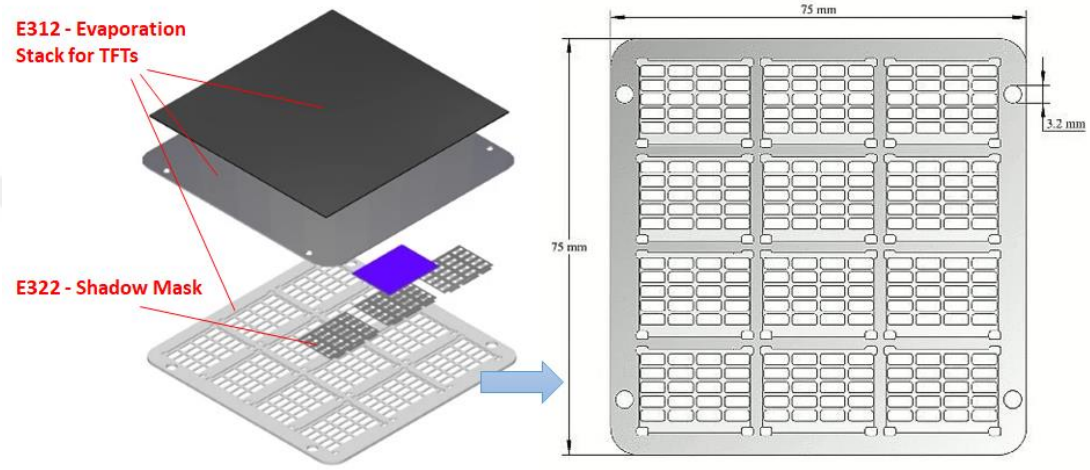


Figure 3.2 Stack configuration of E312 evaporation stack

3.3 Fabrication of Flexible Transparent TFTs

In the production of thin film structures, the sputtering system comes into prominence due to its superior properties such as homogeneous film production, prosess time, production cost, adaptability to large area applications (Evangelou et al., 2003; Mo et al., 2011; Tsui & Chang, 2003; Wasa et al., 2004). Therefore, considering the commercial applicability of this study, all layers of the relevant TFT structure were produced with the sputtering system.

To sustain the glow discharge with an insulator target, rf power supply should be used in related sputtering system instead of dc power supply. This sputtering system is called “Sputter with rf power supply” or “RF sputtering system” (Wasa et al., 2004).

In the 1960s for deposition of dielectric materials on any surface, rf discharge for sputtering method was used as a practical sputtering system (Wasa et al., 2004). A typical sputtering system having RF power supply is shown in Fig. 3.3.

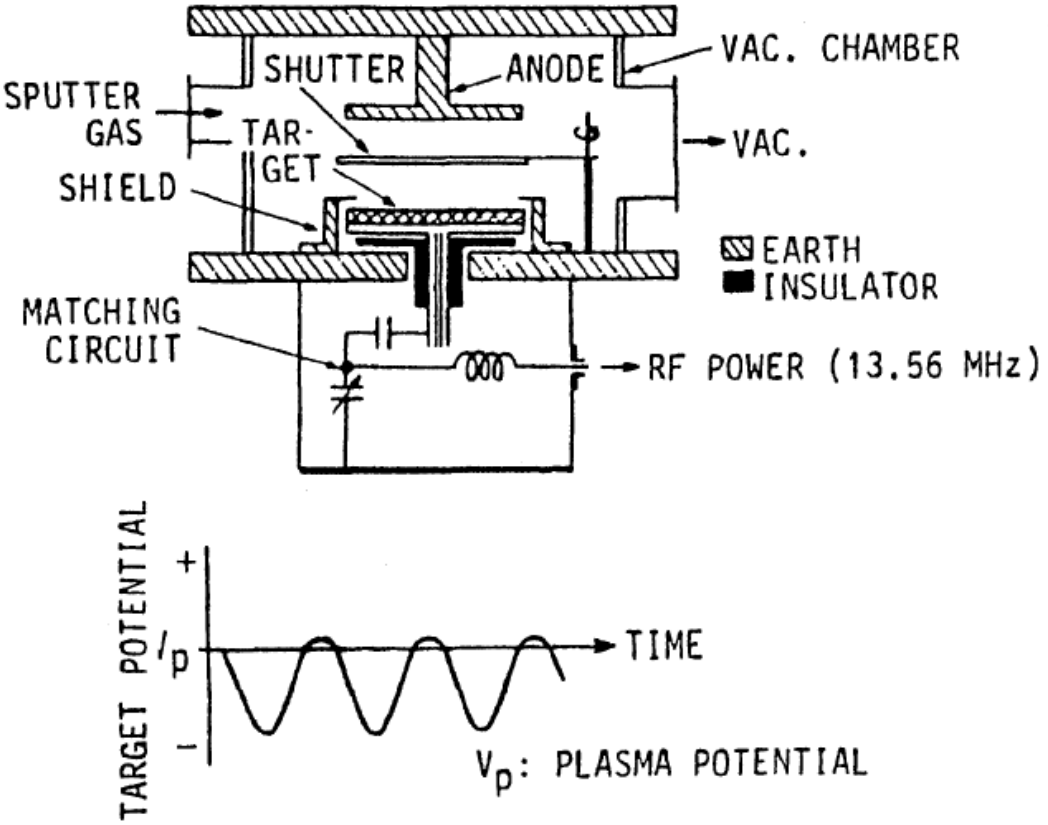


Figure 3.3 Sputtering system with RF power supply (Wasa et al., 2004)

A typical network for impedance matching is shown in Fig. 3.4 (Wasa et al., 2004). In rf diode sputtering, the cathode current density is given by

$$i_s \cong C\frac{dV}{dt} \tag{3.1}$$

In equation 3.1, C value indicates capacitance between the discharge plasma and the target and dV/dt term indicates variations of the target surface potential by time. This means if the frequency of voltage that applies to target increases, the cathode ion currents will increase. In practice, frequency of sputtering system having RF power supply is typically 13.56 MHz.

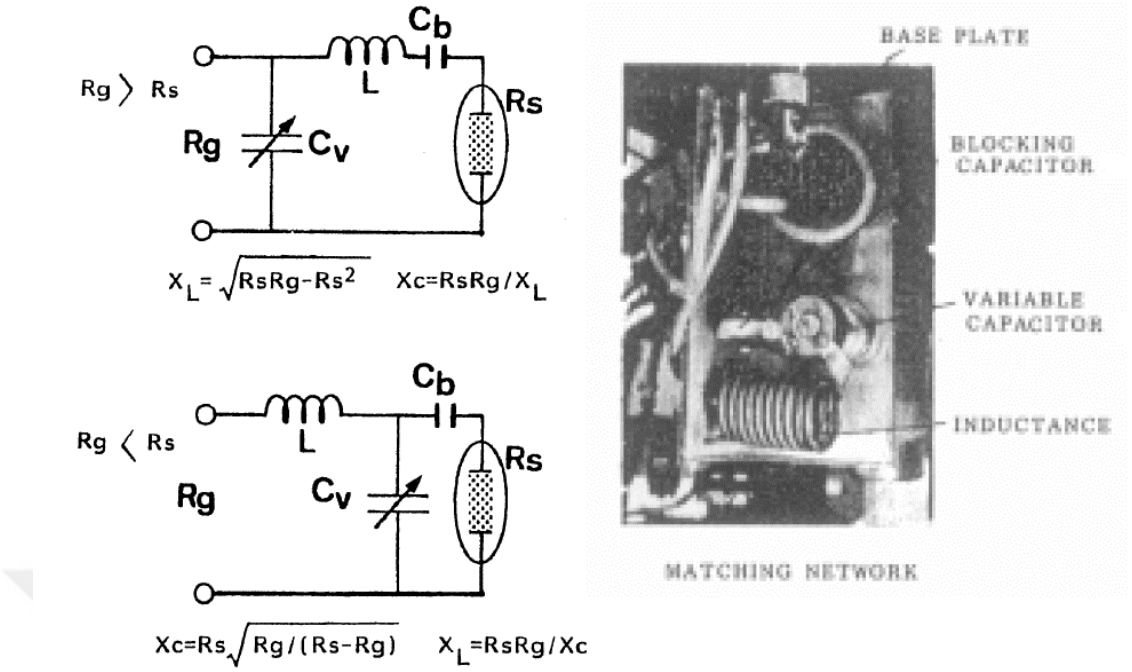


Figure 3.4 Impedance matching networks for sputtering system having RF power supply (Wasa et al., 2004)

The chamber where the deposition process is carried out in sputtering systems is brought to low vacuum values such as 1mTorr in order to prevent the gas ions used for the process and the atoms removed from the target material from interacting with the air monecules. In the sputtering system having RF power supply, a capacitor that is called "Blocking Capacitor" is connected between the matching network and the cathode that is the section into which the target material is placed This anode and cathode configuration is shown in fig. 3.3.

The block diagram of the flexible transparent TFT structure developed in this study is shown in Figure 3.5.

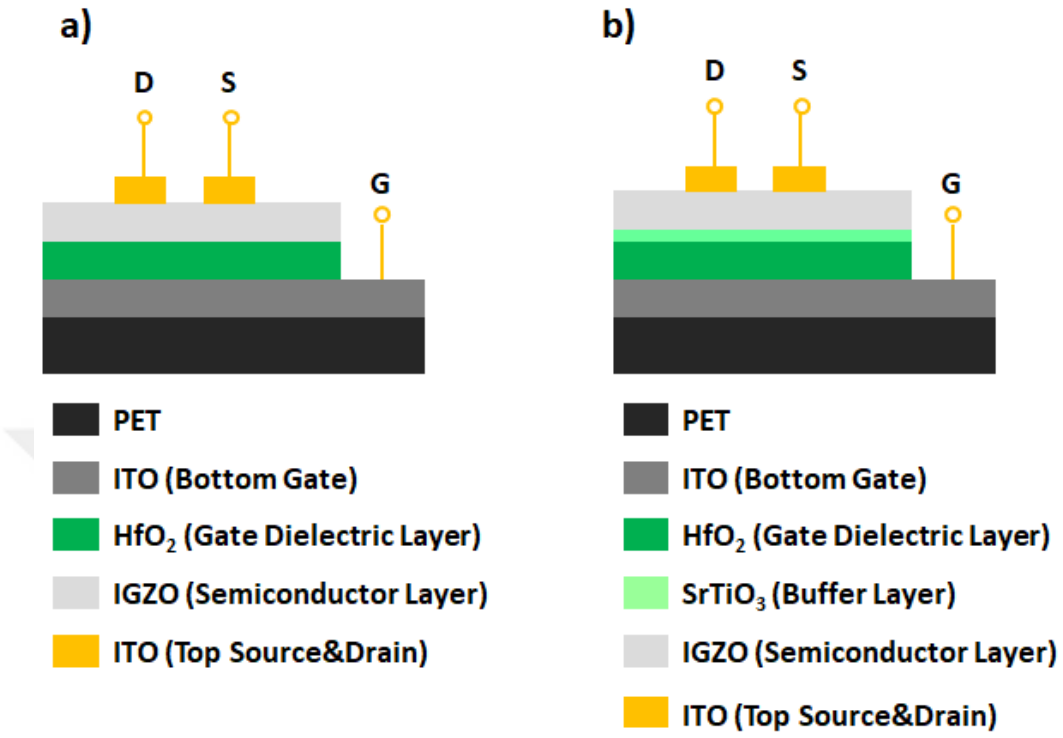


Figure 3.5 flexible transparent TFT structure a) without buffer layer b) with buffer layer

Firstly, thickness calibration of the sputtering system for the fabrication of the relevant layers of flexible transparent TFT device was made for the materials to be used in these layers that is shown in fig. 3.5. Calibration processes for HfO_2, $SrTiO_3$, IGZO and ITO are explained in the work flow diagram in Figure 3.6.

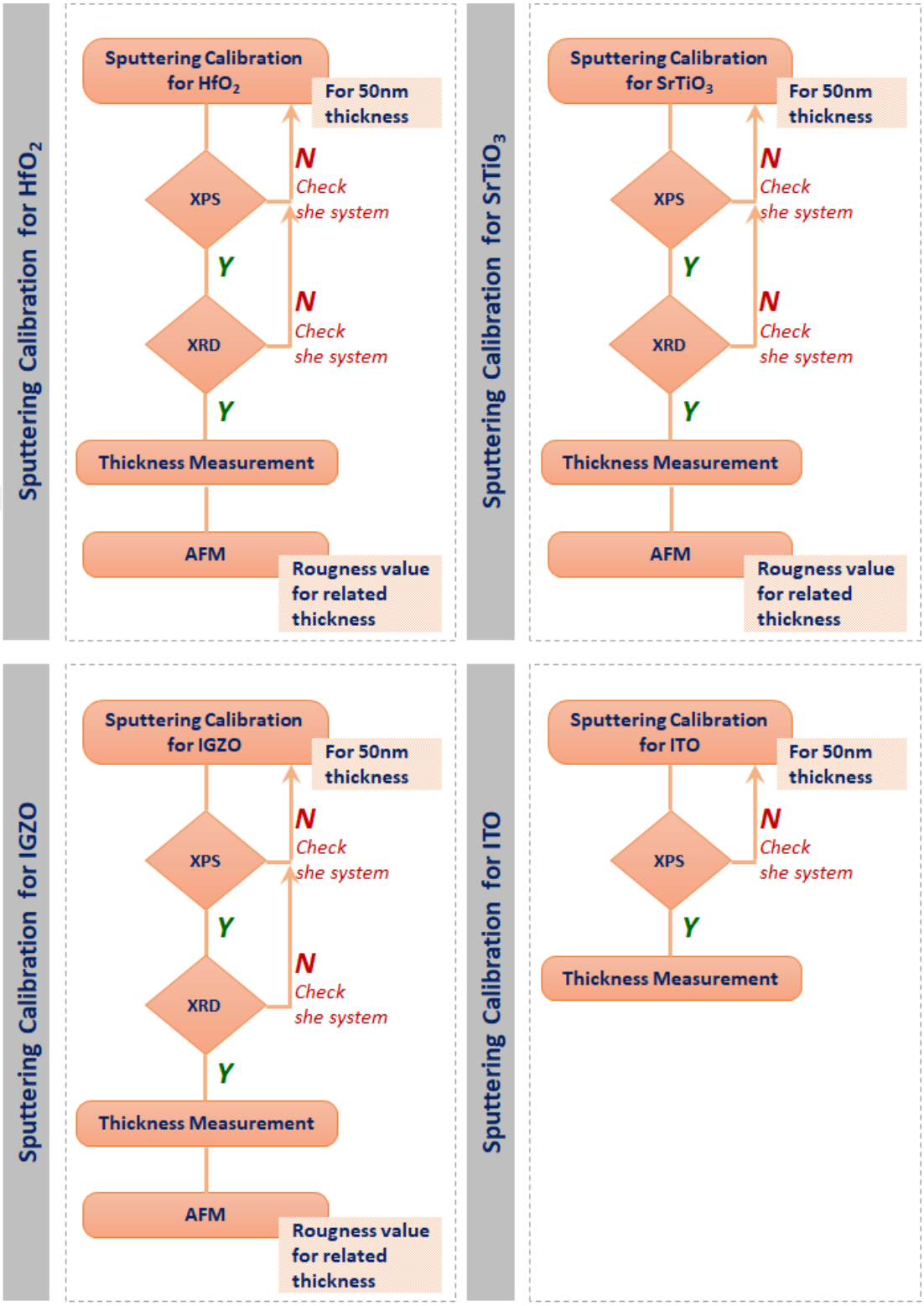


Figure 3.6 Sputtering calibration process for HfO_2, $SrTiO_3$, IGZO and ITO

For the calibration process of HfO_2 shown in Figure 3.6, HfO_2 was deposited on a glass substrate. Before the deposition process, the density, Z-Ratio, tooling and final coating thickness values of HfO_2 were entered to the insitu thickness measurement equipment on the system. Then, 50nm thickness value has been entered in the final coating thickness section. When the system measures 50nm thickness in line with the parameters entered into the insitu thickness measurement equipment, it automatically closes the shutter between cathode and sample and ends the deposition of the relevant material on the sample.

After deposition process, the actual thickness value of the relevant HfO_2 thin film was determined and the new tooling value was calculated with the following equation.

$$New\ tooling\ value = \frac{First\ tooling\ value\ x\ Measured\ thickness\ value}{First\ thickness\ value\ entered\ into\ the\ system} \quad (3.2)$$

The new tooling value calculated in Equation 3.2 is entered into the insitu thickness measurement equipment being on the sputter system, and the thickness calibration of the system for HfO_2 has been completed. After this step, the values read on the insitu thickness measurement system show the actual thickness of the HfO_2 coating. The same process was repeated for thickness calibration of $SrTiO_3$, IGZO and ITO materials. The density, Z-Ratio and tooling values entered into the sputtering system for HfO_2, $SrTiO_3$, IGZO and ITO are given in Table 3.5.

Table 3.5 Density, Z-Ratio and tooling values entered into sputtering system for HfO_2, $SrTiO_3$, IGZO and ITO

TFT Layers	Material	Desnsity (g/cm^3)	Z-Ratio	Tooling
Gate Dielectric Layer	HfO_2	9.68	1.00	250
Buffer Layer	$SrTiO_3$	4.81	0.31	250
Semiconductor Layer	IGZO	6.12	1.00	250
Source-Drain Contacts	ITO	7.14	1.00	250

After the thickness calibration was completed, TFT devices with and without buffer layer for flexible transparent TFT structure were fabricated using the sputtering fabrication parameters shown in Table 3.6.

Table 3.6 Sputtering fabrication parameters for gate dielectric layer, buffer layer, semiconductor layer and Source-Drain contacts

TFT Layers	Symbol	RF Power	Base Pressure	Process Vacuum Level	Final Tooling
Gate Dielectric Layer	HfO_2	60W	$3.00x10^{-6}$Torr	10mTorr	284
Buffer Layer	$SrTiO_3$	50W	$3.00x10^{-6}$Torr	10mTorr	277
Semiconductor Layer	IGZO	25W	$3.00x10^{-6}$Torr	10mTorr	251
Source-Drain Contacts	ITO	30W	$3.00x10^{-6}$Torr	10mTorr	251

E322 model shadow mask and E312 model evaporation stack shown in Figure 3.7 are used to create flexible transparent TFT structures with different channel geometry on substrates prepared in 20mmx15mm dimensions. Substrates are placed on the shadow mask placed in the evaporation stack. Evaporation stack is placed in the sample holder of the sputter system and ITO deposition process for the source-drain contacts is started in this way.

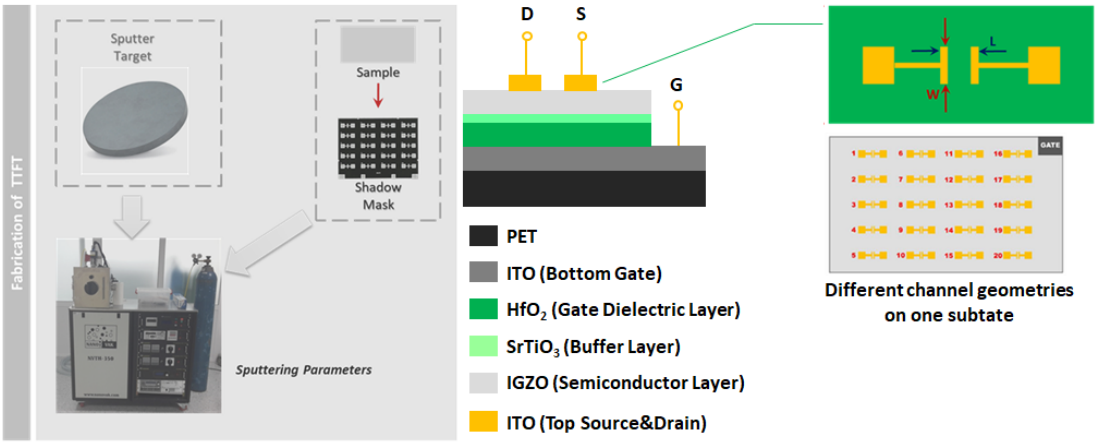


Figure 3.7 Creating different channel geometries on one substrate

The concerning layer thicknesses and channel geometries of the TFT devices developed are shown in Table 3.7.

Tablo 3.7 Layer thickness and channel geometries of developed flexible transparent TFT structures

Device Code	Channel Width	Channel Length	HfO_2 Thickness	$SrTiO_3$ Thickness	IGZO Thickness
TFT-A1	1000 µm	80 µm	40nm	0nm	30nm
TFT-A2	1000 µm	60 µm	40nm	0nm	30nm
TFT-A3	1000 µm	50 µm	40nm	0nm	30nm
TFT-A4	1000 µm	40 µm	40nm	0nm	30nm
TFT-A5	1000 µm	30 µm	40nm	0nm	30nm
TFT-B1	1000 µm	80 µm	40nm	0nm	30nm
TFT-B2	1000 µm	80 µm	40nm	2nm	30nm
TFT-B3	1000 µm	80 µm	40nm	4nm	30nm
TFT-B4	1000 µm	80 µm	40nm	6nm	30nm

3.4 Material Characterizations

3.4.1 Thickness Measurement for Calibration of Sputtering System

The thicknesses of the HfO_2, $SrTiO_3$, IGZO and ITO samples fabricated for the thickness calibration of the sputtering system were determined with the F-20 model thin film thickness measurement system of the "Filmetrics" company shown in figure 3.8.



Figure 3.8 Filmetrics F-20 thin film analysing system

The propagation of light through a film is described by the optical constants *n* and *k*. The electromagnetic field, which describes light passing through a material at a given time, is given as: (Filmetrics, 2022, January 16):

$$A\,cos\left(n\frac{2\pi}{\lambda}x\right)\,exp\left(-k\frac{2\pi}{\lambda}x\right) \tag{3.3}$$

In equation 3.3 *x* is distance traveled by the light in the film , λ is the wavelength of light, *n* and *k* are refractive index and extinction coefficient of related film, respectively. The refractive index is described as the ratio of the light speed in a vacuum to the light speed in concerning material. The extinction coefficient is a measure of how much light is absorbed in the material.

Reflection occurs when light passes through the interface between different materials. The ratio of light reflected by an interface is determined by *n* and *k* (See fig. 3.9). Light reflection from a material in air is defined as (Filmetrics, 2022, January 16):

$$R = \frac{(n-1)^2+k^2}{(n+1)^2+k^2} \tag{3.4}$$

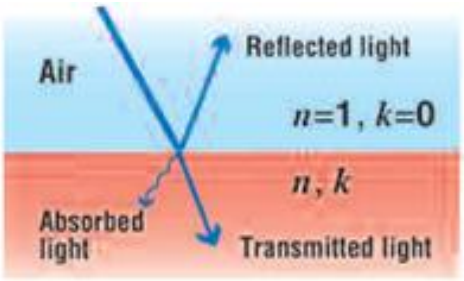


Figure 3.9 Reflection of light from single interface (Filmetrics, 2022, January 16)

First, let's imagine that we are going to measure the optical constants for the simple case of reflected light in a material with a *k* value of 0, using the spectral reflection method. In this case the reflection is (Filmetrics, 2022, January 16):

$$R = \left|\frac{n-1}{n+1}\right|^2 \tag{3.5}$$

In this case, the *n*-value of the materials can be determined by the R measurement. The *n* value of a material varies according to the wavelength. Since reflection is also known at many wavelengths, *n* is also known at each of these wavelengths, as shown in Figure 3.10 (Filmetrics, 2022, January 16).

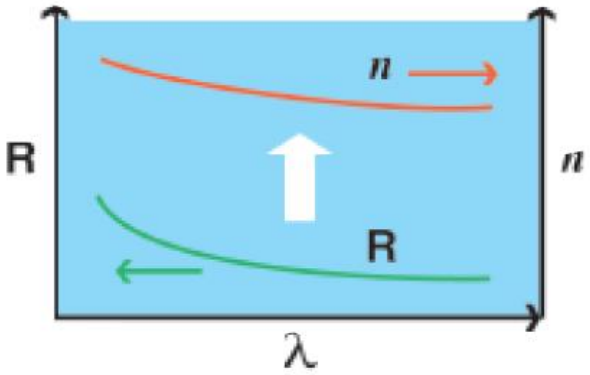


Figure 3.10 Refractive index vs. wavelength (Filmetrics, 2022, January 16)

In another case, a material may have another thin film on it. In this case, the films on both the lower and upper layers of this structure reflect light (See Figure 3.11). The total amount of light reflected from this multi-layered structure is determined as the sum of these two separate reflections. Due to the wave-like nature of light, reflections from two interfaces can come together constructively or destructively, depending on their phase relationship. (Filmetrics, 2022, January 16).

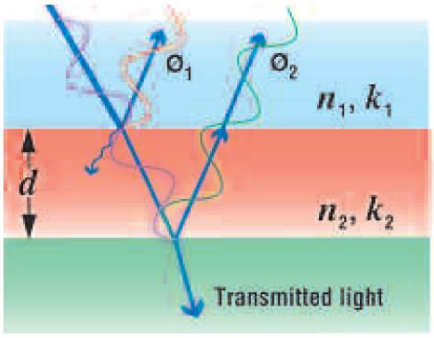


Figure 3.11 Reflection of light from multiple interface (Filmetrics, 2022, January 16)

The phase relations are determined by the difference between the optical path lengths of the two reflections determined depending on the thickness of the relevant film, the optical constants and the wavelength of the light. When the reflections are in phase, the light path is equal to an integer multiple of the wavelength of the light. In this case, constructive interference is obtained. This occurs when $2nd = i\lambda$ when the light comes perpendicularly to a transparent film. In this equation, d is the thickness of the film and i is an integer. On the other hand, reflections are out of phase, If the light path becomes half of a wavelength other than the in-phase condition, or when $2nd = (i+1/2)\lambda$, it is added destructively (Filmetrics, 2022, January 16).

The qualitative aspects of these reflections combined into a single equation are shown below (Filmetrics, 2022, January 16):

$$R \approx A + Bcos\left(\frac{4\pi}{\lambda}nd\right) \tag{3.6}$$

From this, we can see that the reflectance of a thin film will vary periodically with $1/\lambda$, which is illustrated in Figure 3.12. Thicker films produce more oscillations in a given wavelength range. On the other hand, thinner films oscillate less in the same range. It will also often exhibit only part of this oscillation (Filmetrics, 2022, January 16).

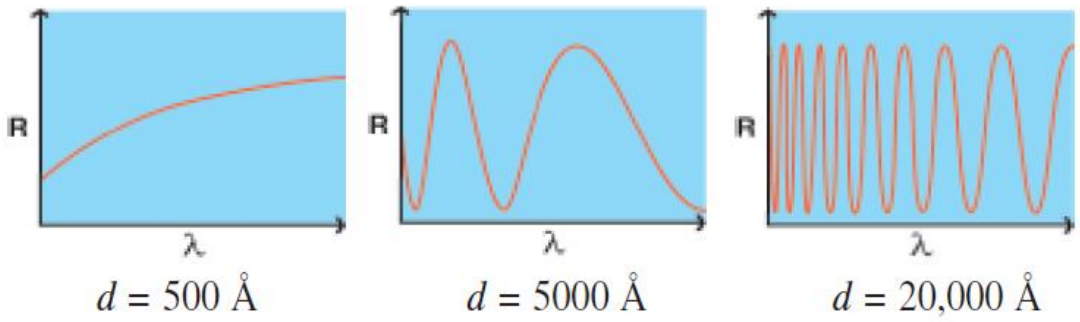


Figure 3.12 Reflection (Filmetrics, 2022, January 16)

The amplitude and periodicity of the reflectance of a thin film is determined by the film's thickness and optical constants such as refractive index.

In this study, the F-20 device was first calibrated with own calibration samples. Then, the refractive indices at 632.8nm of these materials were entered into the F-20 device in order to measure the thickness of the HfO_2, $SrTiO_3$, IGZO and ITO coatings. The refractive indices of HfO_2, $SrTiO_3$, IGZO and ITO materials at 632.8 nm are 1.91, 2.39, 1.85 and 1.86, respectively.

3.4.2 X-Ray Diffraction (XRD)

X-ray diffraction (XRD) analysis method is one of the most basic techniques used (according to Bragg's Law shown in equation 3.7) to determine the crystal structures of different types of materials such as powder, solid and film materials.The XRD device sends an X-Ray to the sample to be analyzed. When X-rays meet the sample, they are refracted and scattered in all directions (Callister & Rethwisch, 2011).

The resulting diffraction distribution gives a map of the crystal lattice structure of the material of interest, and Bragg's law satisfies the condition that a plane wave is refracted by a lattice plane family (Callister & Rethwisch, 2011).

$$n\lambda = 2d(\sin\theta) \qquad (3.7)$$

In equation 3.7, d is lattice spacing, θ is angle between incoming X-Rays and normal of surface, λ its wave length of X-Rays and n is the order of the reflection and it is equivalent to the diffraction condition in reciprocal space and to the Laue equations (Figure 3.13) (Callister & Rethwisch, 2011).

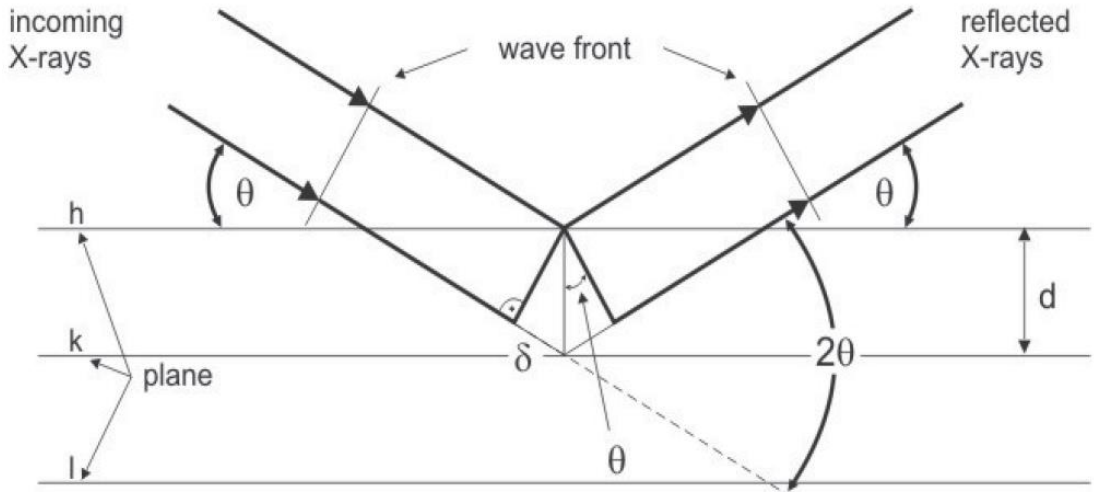


Figure 3.13 The schematic representation of X-ray diffraction (Callister & Rethwisch, 2011)

Crystal structures of related layers on flexible transparent TFT devices were determined by using Thermo Scientific ARL K-alpha X-ray diffractometer. Voltage and current settings of this instrument is 45 kV and 44 mA, respectively and this instrument uses Cu-Kα X-radiation (1.5405 Å). For phase identification of related materilas, XRD spectrums were recorded in the interval $3° \leq 2\theta \leq 90°$ at a speed of 2°/min.

3.4.3 Scanning Electron Microscopy (SEM)

Scanning electron microscopy (SEM) is imaging method used to study the surface morphology and microstructure of solid materials. The surface of the sample to be examined is scanned with high-energy electron beams in the SEM device. The electron beams interact with the sample and thus different types of radiation are produced. SEM device performs the imaging process by analyzing the scattered (backscattered) and removed (secondary) electrons from the sample.Backscattered electrons provide information regarding the composition and topography of the sample surface. Secondary electrons are used to show details concerning the surface morphology of related material (Yıldırım, 2017). Figure 14 shows the basic structure of a typical SEM device schematically.

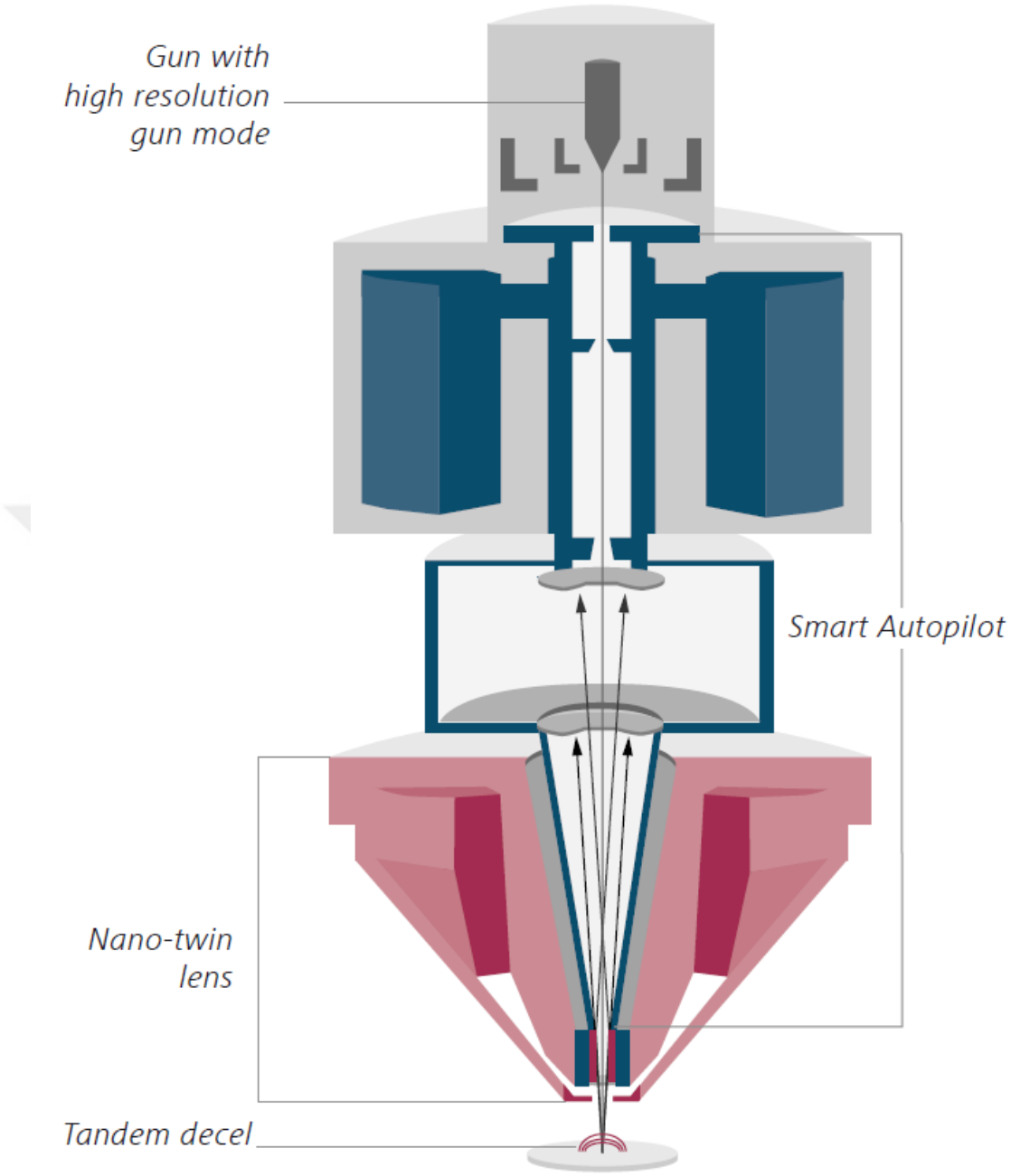


Figure 3.14 The schematic representation of SEM (Zeiss, 2022)

To verify the production method, HfO_2, $SrTiO_3$, and IGZO thin films were first produced on a glass substrate before SEM (ZEISS GeminiSEM 560 SEM) analysis. The surface qualities of HfO_2, $SrTiO_3$, and IGZO thin films on Glass substrates were examined by using SEM (ZEISS GeminiSEM 560 SEM).

3.4.4 Surface Analysis of Concerning Layers - X-Ray Photoelectron Spectroscopy (XPS)

"X-ray photoelectron spectroscopy (XPS) is a surface analysis method used to determine the basic composition of the elements on a material surface, the chemical formula of the relevant molecules, the bond structures and electronic states of the relevant atoms. XPS spectra are obtained by measuring electrons escaping from 1 to 10 nm from the surface of the material as a result of bombardment of the surface of concerning material with low energy X-Rays (Figure 3.15). XPS requires ultra-high vacuum (UHV) conditions (Yıldırım, 2017). If the atomic number of the element to be analyzed is 3 or greater, these elements can be analyzed with XPS. The probability of detecting electrons to be removed from these elements as a result of the photoelectric event is almost zero. Additionally, it is a routinely used method for surface analysis of all solid materials (Yıldırım, 2017).

Monochromatic Al-Kα (1486.7 eV) X-ray was used in the XPS system (Thermo-Scientific K-Alpha) used to determine the elemental composition and surface chemistry of all samples, and the diameter of the X-ray beam was adjusted to 400 nm. The device is calibrated according to the gold. Pressure was kept below $5x10^{-10}$ mbar during spectral data collection. The XPS data for survey scan mode were scanned from -10 to 1350 eV applying 150 eV transition energy and 1 eV resolution. 20 scans were recorded from a single point. XPS spectra revealed binding energies of Hf4f, O1s, Sr3d, Ti2p, Zn2p3, Ga2p3 and In3d5. 30 eV as pass energy value was used for high resolution elemental scaning mode. The scan number was accepted as 15. Binding energies of electrons for related atoms and deconvoluted spectra were obtained using the curve fitting program that is called "Thermo Avantage V5.65" provided by Thermo Scientific Company (Yıldırım, 2017).

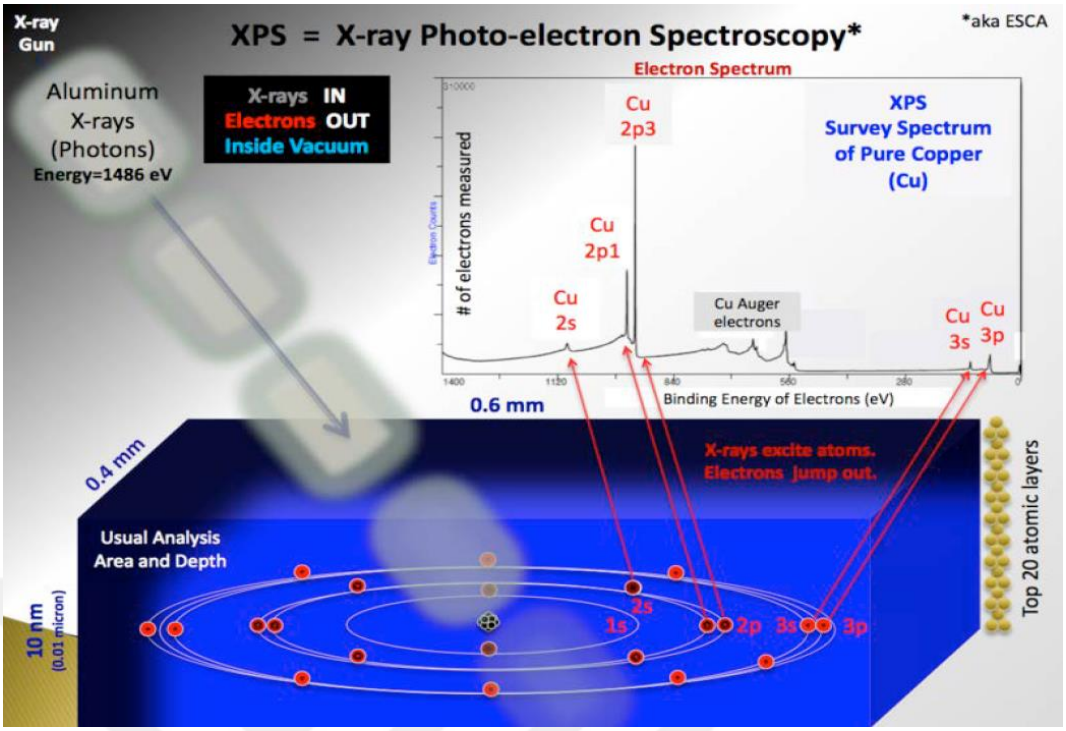


Figure 3.15 Schematic illustration of working principle of XPS (Yıldırım, 2017)

Another important application of XPS analysis is that it provides the opportunity to make surface analysis based on depth. In this thesis study, the atomic interactions occurring while the surface modification made on the gate dielectric layer contributes to the electrical performance of the relevant TFT device was investigated by XPS depth analysis. The surface of TFT devices was bombarded with argon ions and the surface of TFT devices modified with $SrTiO_3$ and not modified with $SrTiO_3$ was analysed from 5nm, 15nm and 25nm depths respectively, and the percentage of oxygen atoms bonded with metal atoms and not bonded at the interface between the gate dielectric layer and the semiconductor layer was determined.

3.4.5 Determination of Surface Morphology of Related Layers - Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) is a microscopic imaging method that is often used to determine the surface morphology and 3D surface topography of thin films. Nanosurf easyScan 2 AFM system was used in tapping mode to determine the surface morphology of thin films. In the "Tapping Mode" technique, the AFM head on which the probe is attached moves on the surface while scanning, the probe oscillates at a

fixed frequency. The oscillation amplitude of the probe varies with the surface morphology of the film, and this change is used to establish the surface morphology of the film and determine the surface roughness (Birlik, 2011). The AFM was well calibrated for z-axis movement.

In addition, the average surface roughness values (Sa) for the relevant samples were determined. The measuring area of all samples is 5 μm and the analysis parameters for the AFM system were also determined as 5 seconds time/line rate and 512 dots/line resolution.

3.5 Optical Characterizations of Flexible Transparent TFTs

UV-VIS spectroscopy method is a molecular spectroscopy method that is frequently used to determine the absorption and transmittance values of liquid samples in the UV-VIS wavelength range. The block diagram of a basic UV-VIS spectrophotometer system is shown in Figure 3.16 (Rocha et al., 2018).

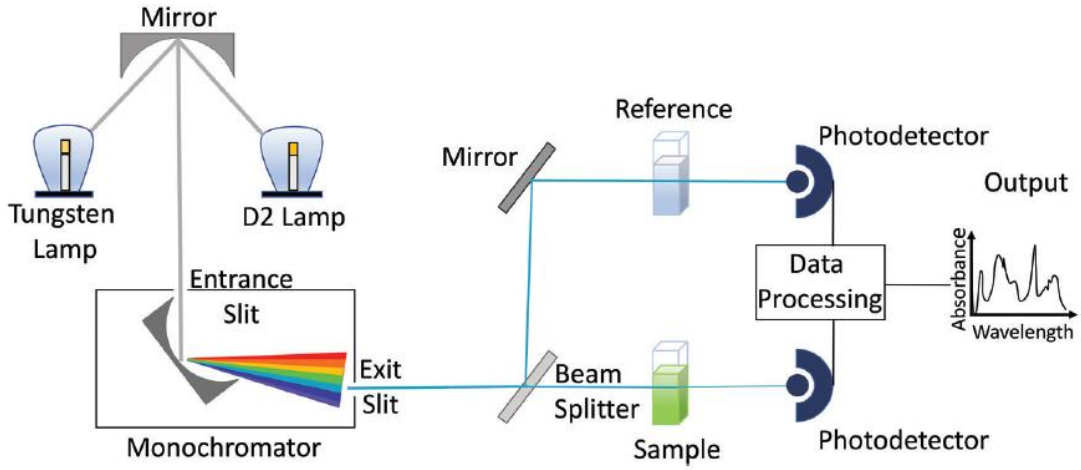


Figure 3.16 UV-vis spectrophotometer diagram with double beam configuration (Rocha et al., 2018)

In order to determine the optical transmittance values of solid or film samples in the UV-VIS wavelength range, the relevant measurement systems are modified with different apparatus. An example of this is the evolution 600 model UV-Vis system of "Thermo Scientific" company at Dokuz Eylul University, EMUM. This system has been modified with a special integrating sphere. In this way, it can make optical measurements of film samples in the UV-VIS wavelength range (See fig. 3.17).

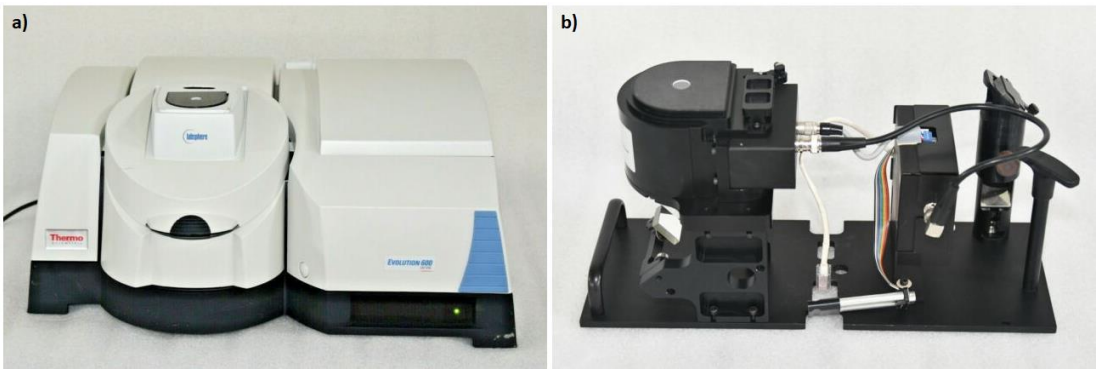


Figure 3.17 “Thermo Scientific” a) evolution 600 UV-Vis spectrophotometer and b) integrating sphere attachment

The optical transmittance spectra between 300-700nm of the flexible transparent TFTs produced in this study were determined using the UV-VIS system shown in Figure 3.17.

3.6 Reliability Tests for TFTs

Resistance to environmental conditions of products developed in display technologies is one of the most important acceptance conditions. In this context, all of the products developed for display technologies are exposed to different temperatures and different humidity values for a certain period of time and their performance under these conditions is tested. The most important of these tests are thermal cycle test (TCT), thermal shock test (TST) and high temperature high humidity (HTHH) tests (Ozer et al., 2022).

After the TFT structure with the best electrical performance developed in this study is placed in the experimental layout shown in Figure 3.17. TCT, TST and HTHH tests were applied to this TFT in design quality asuerance department in VESTEL Electronic company. The electrical performance of the related product has been determined before and after the test (Ozer et al., 2022).

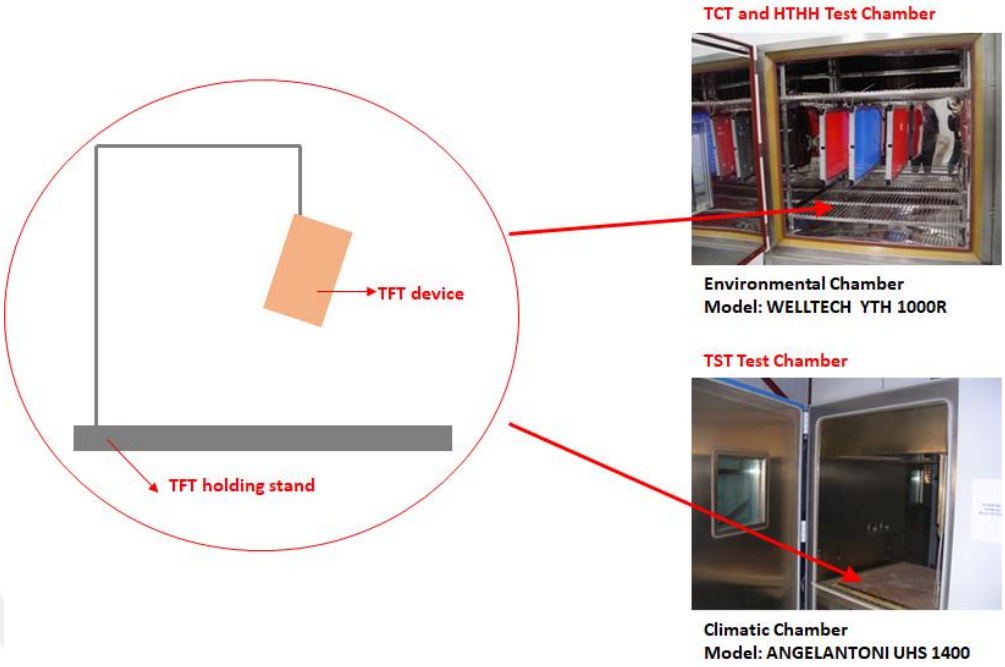


Figure 3.18 Experimental test setup of TFT device for reliability tests at VESTEL Electronic company

3.6.1 Thermal Cycle Test (TCT)

To test the TFT function is still acceptable under various temperature & humidity environments. Product may be stored in varied temperature & humidity environments during the transportation process, so it must be tested to verify its temp/humidity endurance. TCT test is applied as 2 cycles. The temperature and humidity conditions of the TCT test applied for TFT are shown in Figure 3.19.

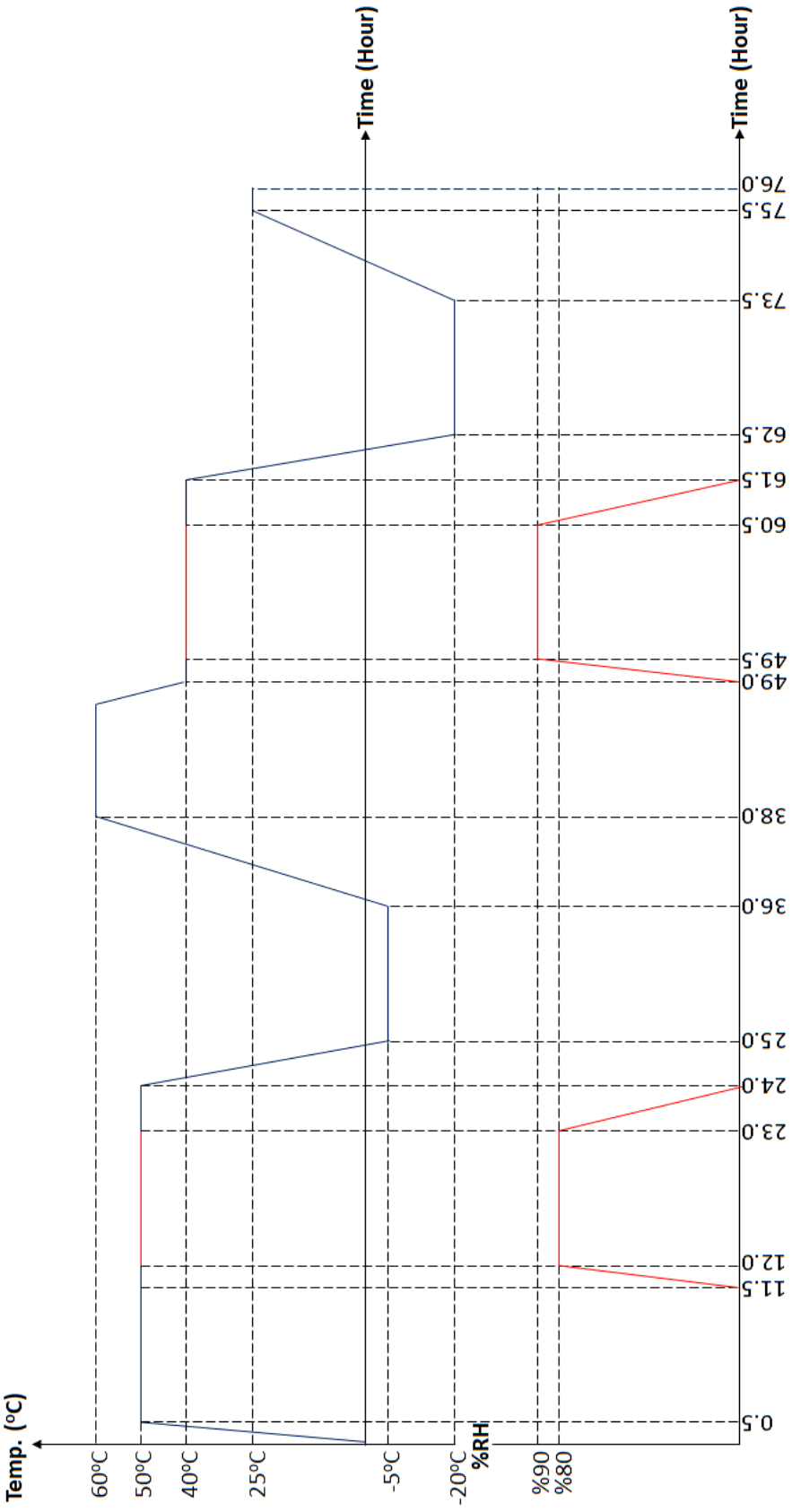


Figure 3.19 Temperature and humidity conditions for TCT test

TCT test was applied using “WELLTECH” YTH 1000R model test chamber (See fig. 3.20) in VESTEL, Design Quality Assurance (DQA) department.



Figure 3.20 “WELLTECH” YTH 1000R environmental chamber at VESTEL Electronic company

3.6.2 Thermal Shock Test (TST)

This test was applied to TFT device to verify thermal shock effect on this structure. TCT test is applied as 200 cycles. The temperature and humidity conditions of the TCT test applied for TFT are shown in Figure 3.21.

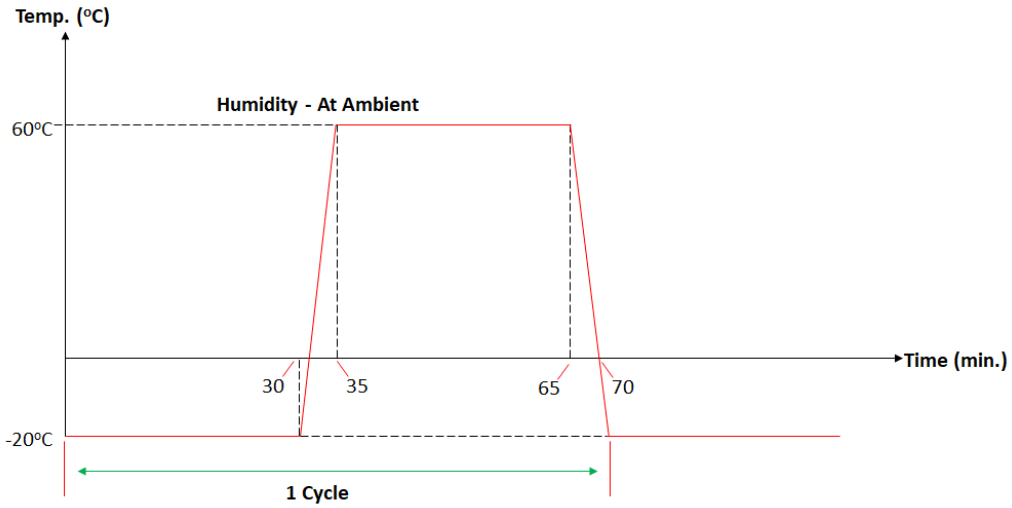


Figure 3.21 Temperature conditions for TST test

TST test was applied using “ANGELANTONI” UHS 1400 model test chamber (See fig. 3.22) in VESTEL, Design Quality Assurance (DQA) department.



Figure 3.22 “ANGELANTONI” UHS 1400 climatic chamber at VESTEL Electronic company

3.6.3 High Temperature High Humidity Test (HTHH)

This test was applied to TFT device to verify high temperature and high humidity effect on electrical performance of this structure. HTHH test is applied during 500 hours. The temperature and humidity conditions of the HTHH test applied for TFT are shown in Figure 3.23.

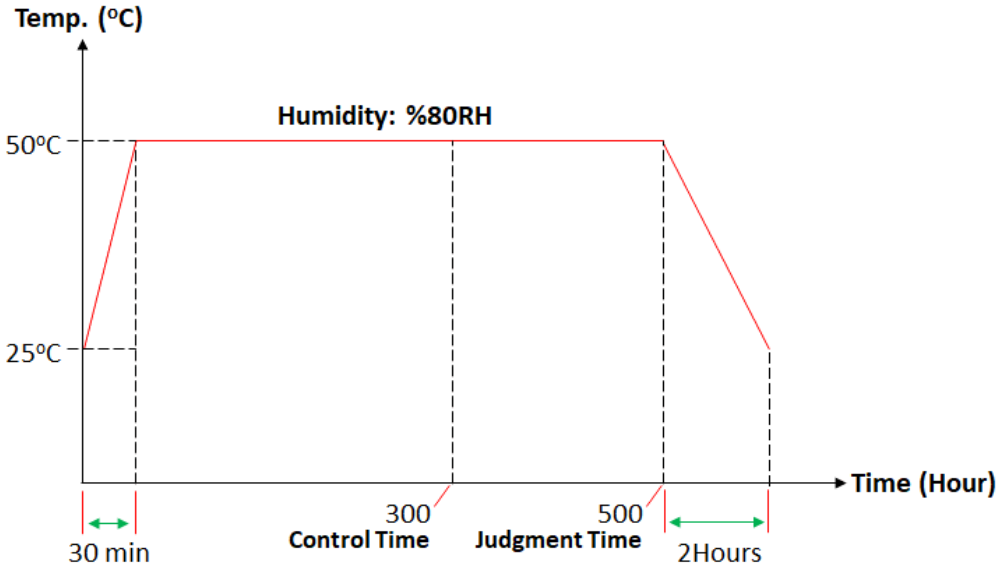


Figure 3.23 Temperature and humidity conditions for HTHH test

HTHH test was applied using “WELLTECH” YTH 1000R model test chamber (See fig. 3.24) in VESTEL, Design Quality Assurance (DQA) department.



Figure 3.24 “WELLTECH” YTH 1000R environmental chamber at VESTEL Electronic company

3.7 Electrical Characterizations of TFTs

The electrical characterization of the flexible transparent TFT structure developed in this study was carried out in Bilkent-UNAM using a keithley 4200 semiconductor parameter analyzer connected to a probe station.

In order to calculate the μ_{FET}, V_{th}, $I_{leakage}$ and I_{on}/I_{off} values of TFT structures, it is necessary to determine the transfer curve of the relevant TFT structure shown in figure 3.25.

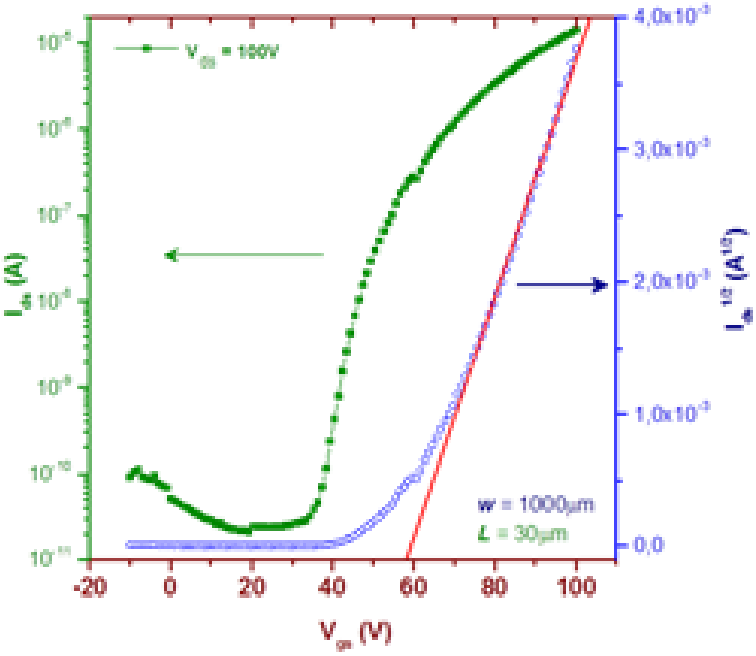


Figure 3.25 Transfer curve of the TFT devices

For the TFT structures produced in this study, a V_g vs I_{ds} graph was created at a constant V_{ds} voltage. The current-voltage characteristic of a transistor in the saturation region is expressed by equation 3.8 below.

$$(I_{ds})_{sat} = \left(\frac{W}{2L}\right)\mu_{FET}C_i\left(V_{gs} - V_{th}\right)^2 \tag{3.8}$$

Equation 3.9 is obtained by taking the square root of Equation 3.8.

$$\sqrt{(I_{ds})_{sat}} = \sqrt{\left(\frac{W}{2L}\right)\mu_{FET}C_i}\,(V_{gs}) - \sqrt{\left(\frac{W}{2L}\right)\mu_{FET}C_i}\,(V_{th}) \tag{3.9}$$

- W: Active channel width of the corresponding transistor (cm)
- L: Active channel length of the corresponding transistor (cm)
- C_i: Capacitance value per unit area of the dielectric layer (F/cm^2)
- μ_{FET}: Fet mobility value of the relevant transistor (cm^2/V.s)

For the region that shows a linear increase where the blue graph shown in Figure 3.25, a linear line is created by using the "Linear Curve Fitting" method (See fig. 3.26). The equation of this newly plotted line is shown below by equation 3.10.

$$y = ax + b \tag{3.10}$$

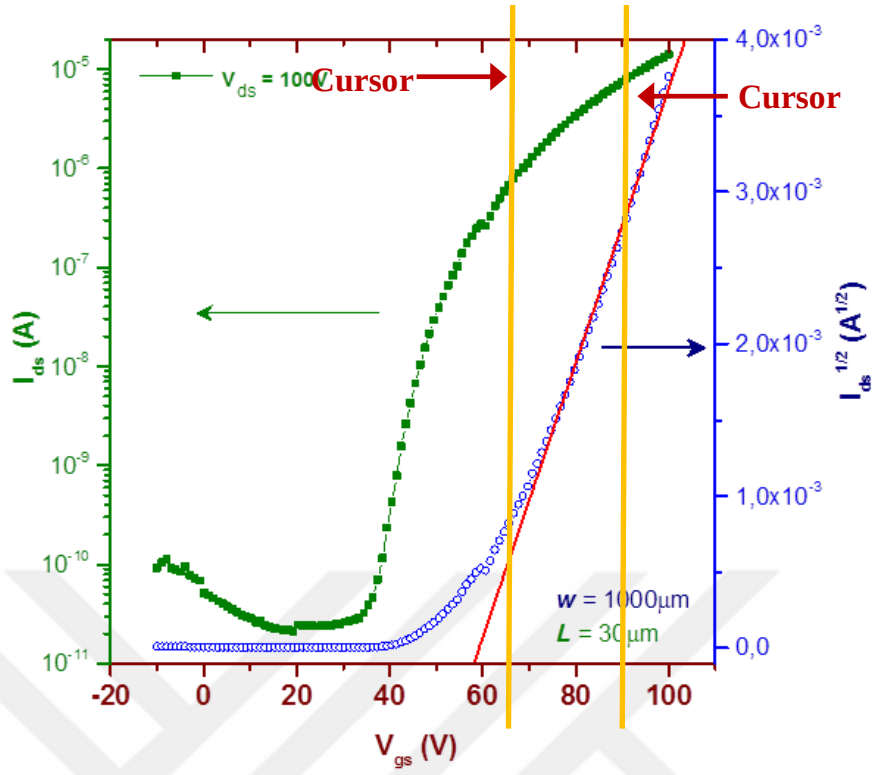


Figure 3.26 Selection of related region on transfer curve of TFT for calcultion of μ_{FET} and V_{th}

As a result of the curve fitting process, "a" and "b" parameters in equation 3.10 are found. μ_{FET} and V_{th} values are calculated from the following equations.

$$a = \sqrt{\left(\frac{W}{2L}\right)\mu_{FET}C_i} \;\; ; \;\; \boldsymbol{\mu_{FET}} = a^2\left(\frac{2L}{W}\right)\frac{1}{c_i} \tag{3.11}$$

$$(\boldsymbol{V_{th}}) = -\,{}^{b}/_{a} \tag{3.12}$$

As shown in Figure 3.27, I_{ds} current cannot flow through the active channel until the TFT structure exceeds the V_{on} gate voltage value. However, even if the gate voltage of the TFT structure is below the V_{on} value, a small amount of leakage current may flow through the active channel depending on the magnitude of the applied V_{ds} voltage. This value is called as the $I_{ds\text{-}leakage}$ current value. $I_{ds\text{-}leakage}$ value is the maximum current that can flow through the source-drain at the value where the gate voltage is lower than V_{on}. To calculate this value, the average of the current values remaining between the region shown in Figure 3.27 is taken. This value gives us the source-drain leakage current value.

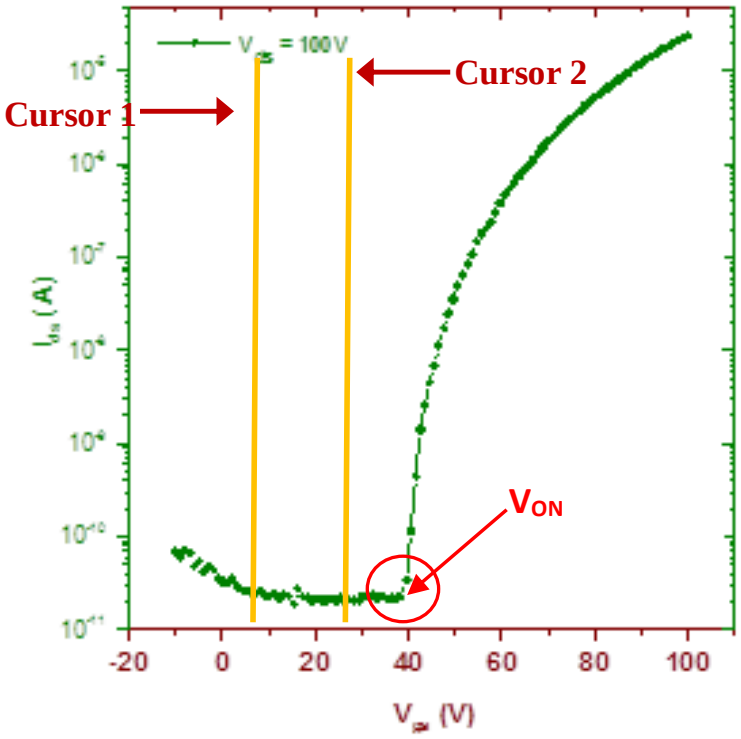


Figure 3.27 Determination of Source-Drain leakage current

For the I_{On}/I_{Off} ratio, the current values of the relevant transistor, I_{ds1} and I_{ds2}, shown in Figure 3.28, were determined. Then, the I_{On}/I_{Off} ratios of developed TFT structures in this study were calculated as in the equivalence 3.13.

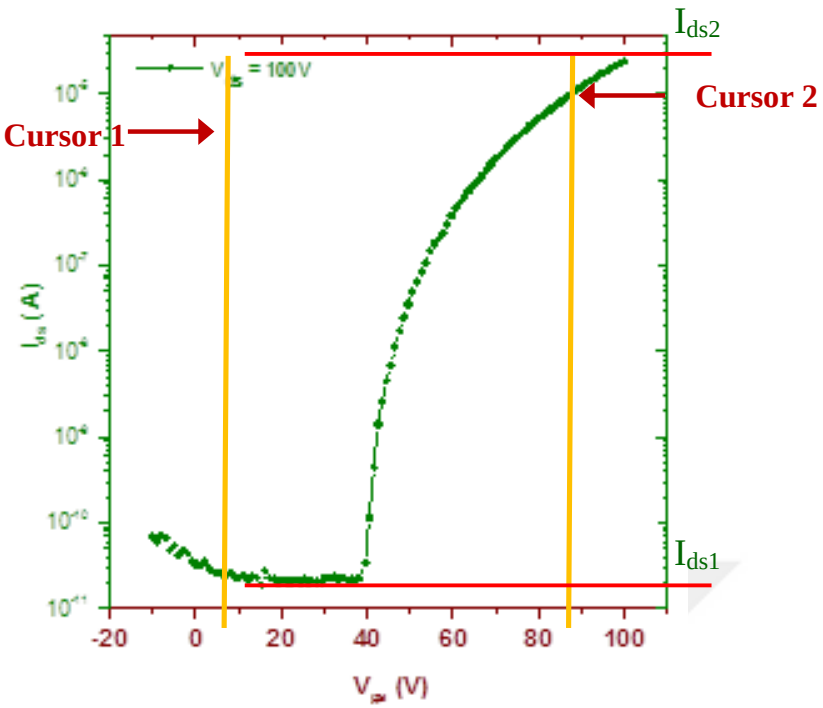


Figure 3.28 Determination of I_{on}/I_{off} ratio

$$\boldsymbol{I_{on}/I_{off}} = \frac{I_{ds2}}{I_{ds1}} \tag{3.13}$$

CHAPTER FOUR

RESULTS AND DISCUSSION

4.1 Results of Material Characterizations

4.1.1 Thickness Measurement for Calibration of Sputtering System

The results of the thickness measurements performed with the "Filmetrics" F20 thickness measurement system of HfO_2, $SrTiO_3$, IGZO and ITO thin films produced on glass substrate for the verification of the thickness calibration and fabrication parameters of the sputter system are shared in figures 4.1, 4.2, 4.3 and 4.4. Measurements were made from 10 different points of the thin films that were produced.

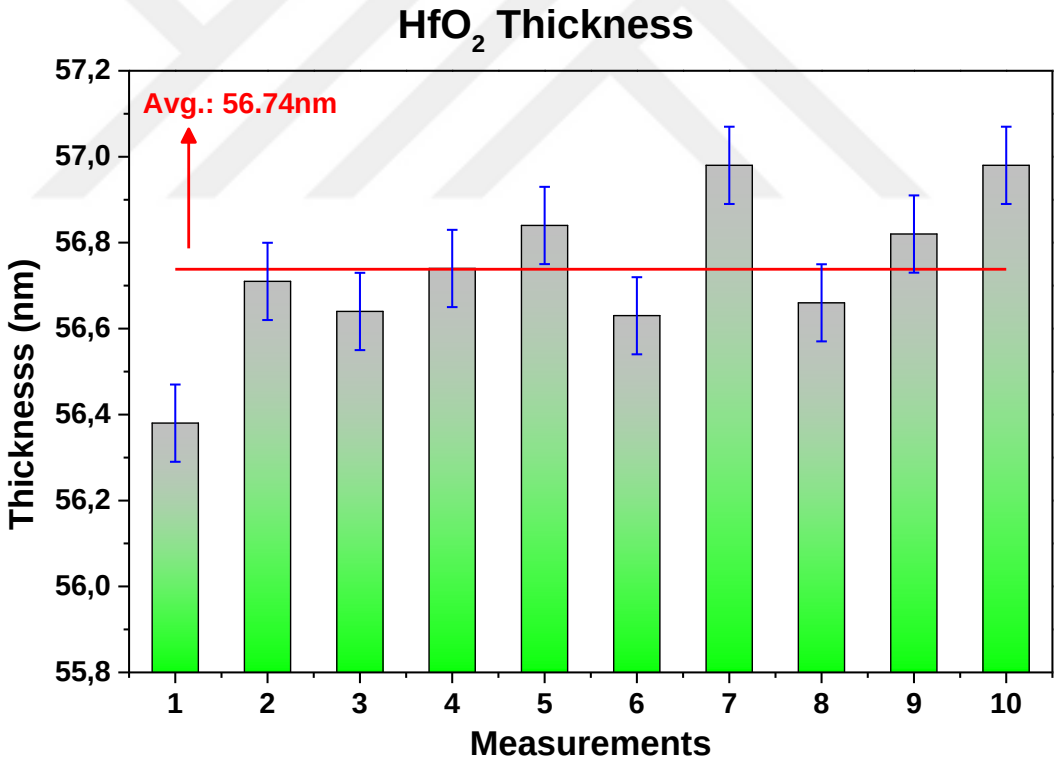


Figure 4.1 Thickness results of HfO_2 thin films

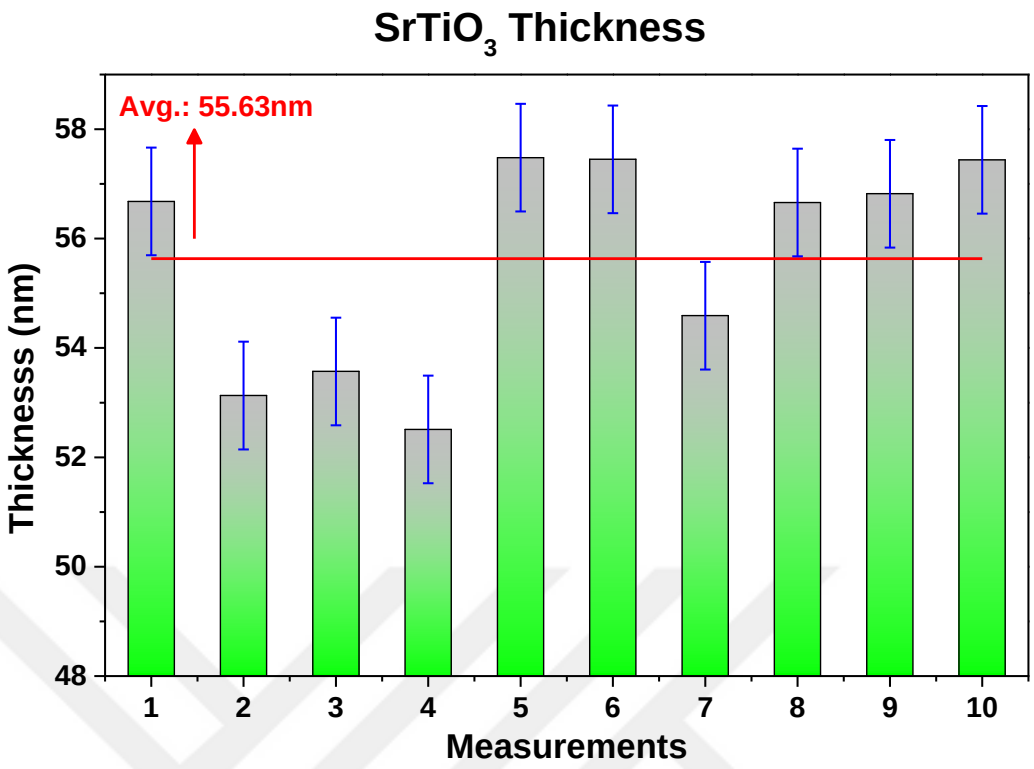


Figure 4.2 Thickness results of $SrTiO_3$ thin films

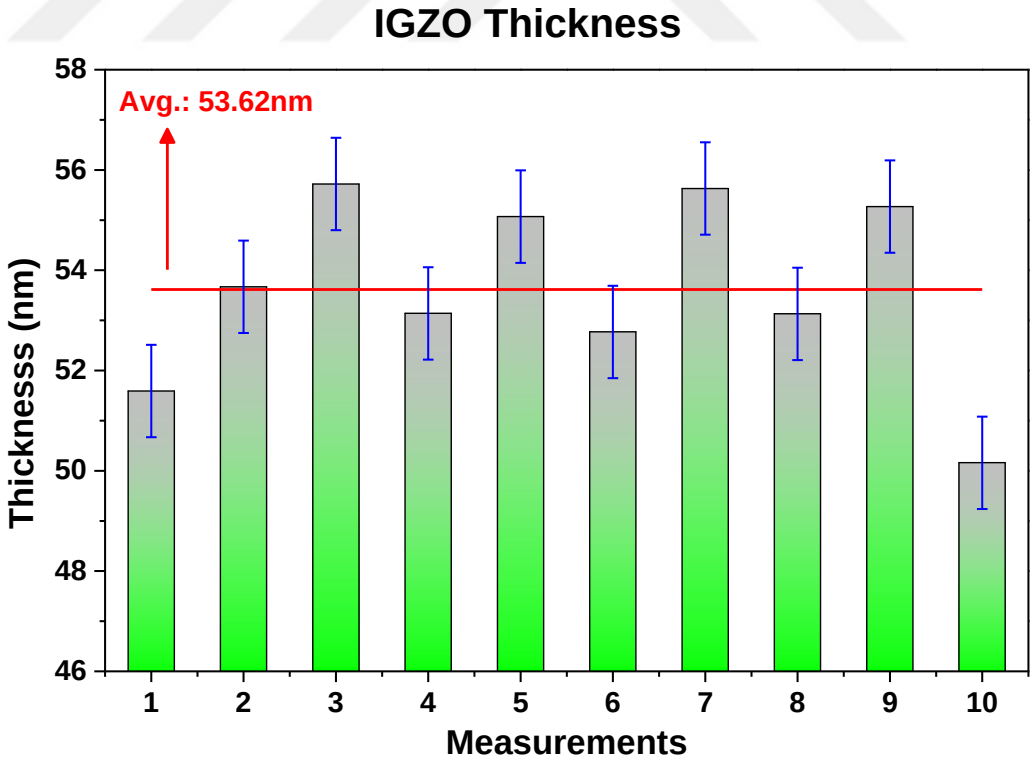


Figure 4.3 Thickness results of IGZO thin films

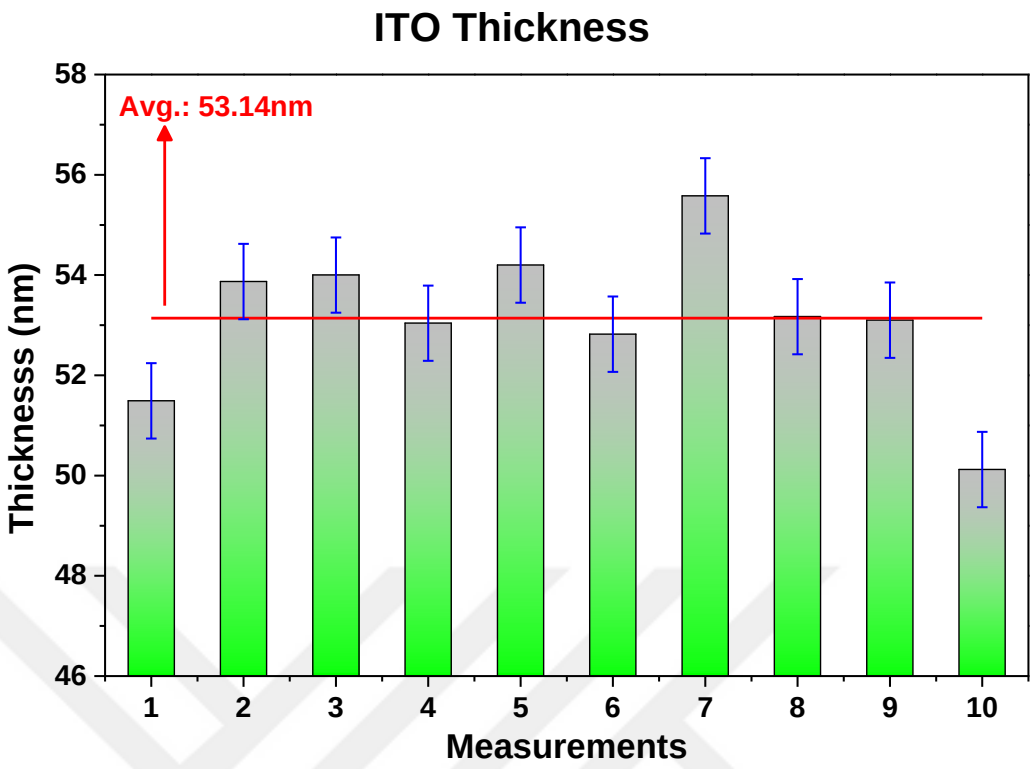


Figure 4.4 Thickness results of ITO thin films

After the thickness measurements, the new tooling values shown in Table 4.1 are calculated for the relevant materials. Then, these new tooling values were entered into the thickness measurement equipment of the sputter system and the thickness calibration of the system was completed. In addition to this, the low standard deviations of the thickness measurement values made from different points of the fabricated films indicate that film fabrication can be uniformly achieved.

Table 4.1 Calculated tooling values for thickness calibration of sputter system

Layer	Entered Film Thickness to Sputter System	Measured Avg. Film Thickness	First Tooling	Final Tooling
HfO_2	50nm	56,74nm	250	284
$SrTiO_3$	50nm	55,43nm	250	277
IGZO	50nm	53,61nm	250	251
ITO	50nm	53.14nm	250	251

4.1.2 Structural Analysis by XRD and SEM

In this study, another important characterization step to verify the production parameters of HfO_2, $SrTiO_3$ and IGZO thin films is XRD analysis. The results of XRD analysis of HfO_2, $SrTiO_3$ and IGZO thin films that will respectively form the gate dielectric layer, buffer layer and semiconductor layer of the relevant TFT structure are shown in figures 4.5, 4.6 and 4.7.

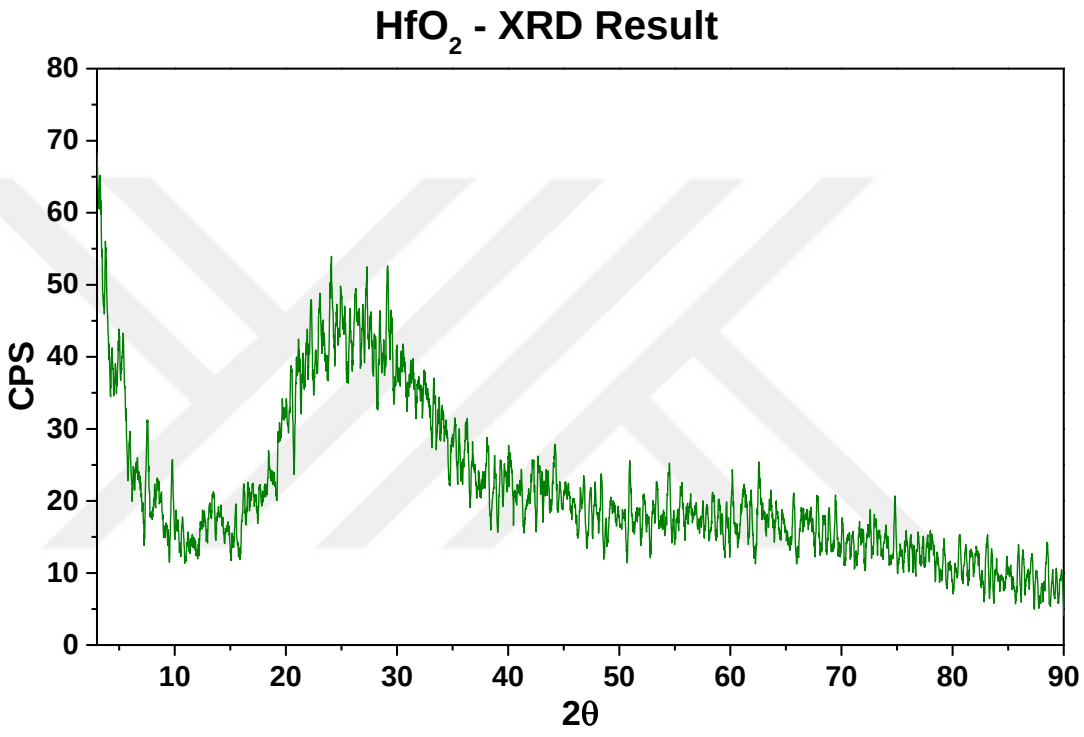


Figure 4.5 XRD spectrum of HfO_2 thin films

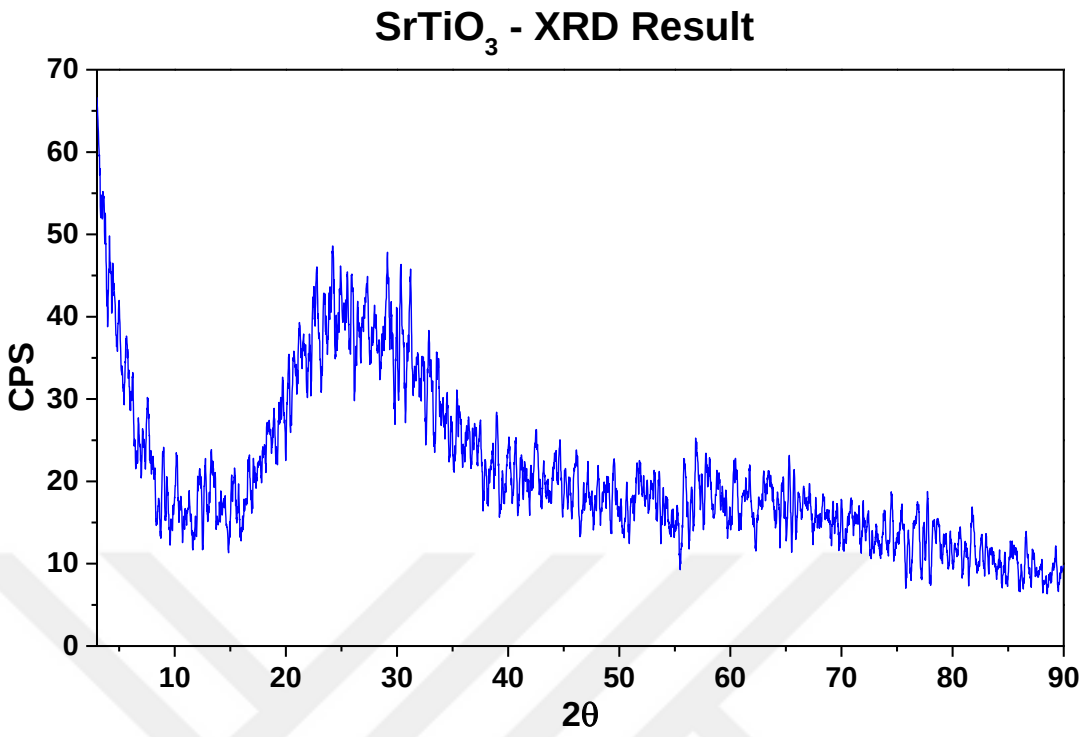


Figure 4.6 XRD spectrum of $SrTiO_3$ thin films

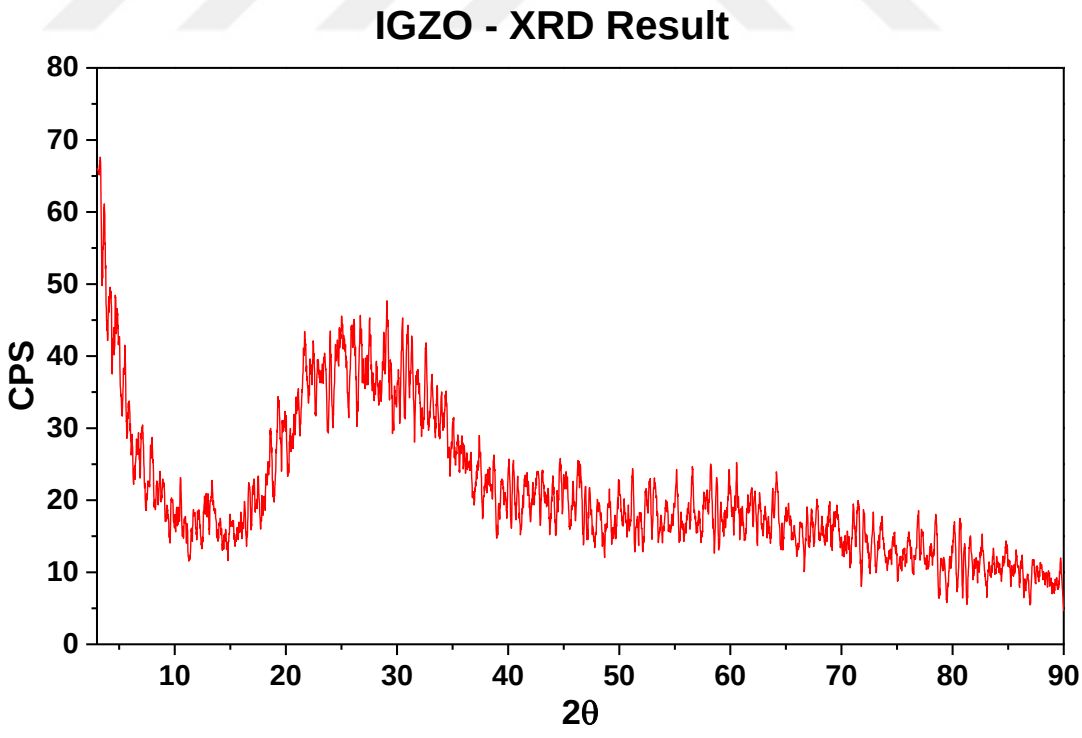


Figure 4.7 XRD spectrum of IGZO thin films

Considering the related XRD results, it is seen that HfO_2, $SrTiO_3$ and IGZO thin films have amorphous phase. These results showed that all layers of the flexible transparent TFT structure can be produced in amorphous structure with the relevant sputtering production method and parameters. In line with these results, the sputtering fabrication parameters that will allow to produce all layers of the relevant TFT structure in amorphous phase were determined.

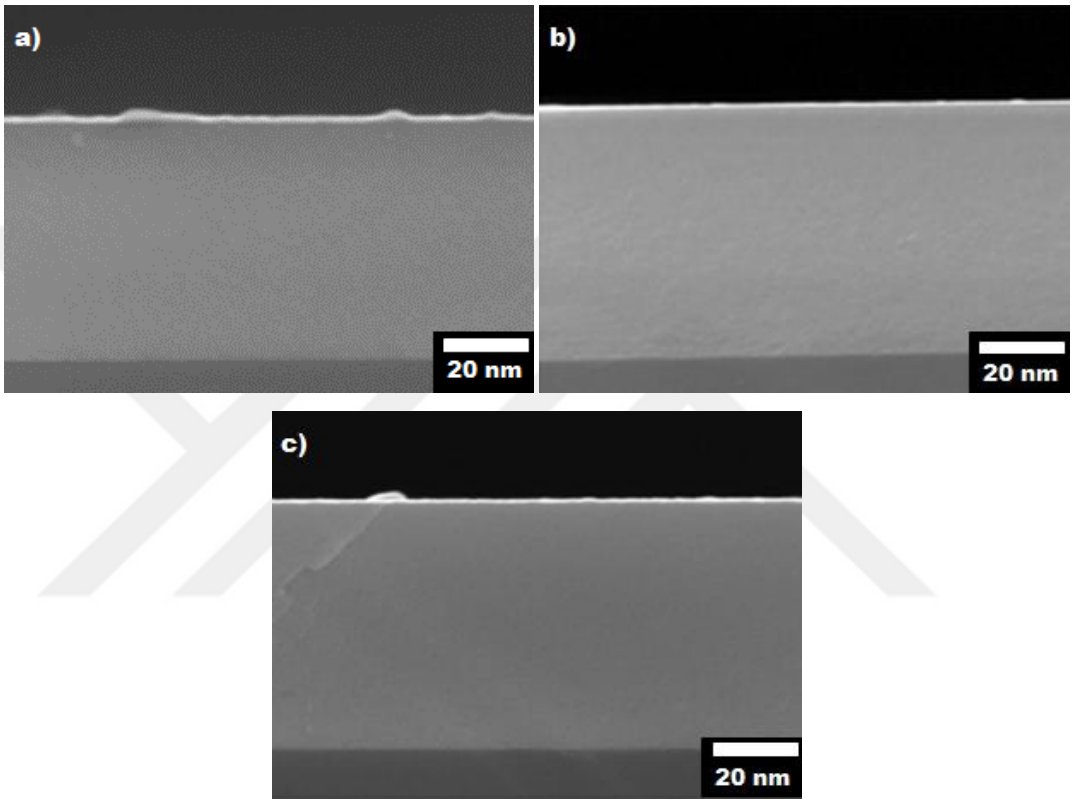


Figure 4.8 SEM images of the cross section morphology of a) HfO_2, b) $SrTiO_3$ and c) IGZO thin films on glass substrate deposited by sputtering method

Cross-section morphology of the deposited thin films were analyzed using scanning electron microscopy as shown in Figure4.8. Both XRD results and the cross-section images of HfO_2, $SrTiO_3$ and IGZO thin films confirmed that they have smooth, crack free micro structure and also that they have no grain boundary. The important result obtained here is that the relevant layers of the TFT structure that is produced do not have grain boundaries. It is known that the grain boundaries are the points where electrons are likely to be trapped (Fan et al., 2019; Hsieh et al., 2010; Ozer et al., 2022; Rembert et al., 2015). The amorphous production of the relevant layers of the TFT

device reduces the possibility of trapping electrons in the surface where they move. This means that the electrical performance of the relevant TFT device increases. Another advantage of the amorphous production of all layers of TFT is that this structure can be produced ultra-smooth in large areas (Fortunato et al., 2010; Gogoi et al., 2015; Gutierrez-Heredia et al., 2017; Hsu et al., 2013; Jang et al., 2015; Ozer et al., 2022). This makes it possible to use this TFT structure in large-scale applications such as display technologies without any decrease in its performance.

4.1.3 Elementel Analysis with XPS

XPS analysis was performed to determine the chemical composition and oxidation states of the respective thin films formed on glass substrates for thickness calibration of sputter system and production method verification. Survey spectrum and high resolution elemental scaning results of the produced HfO_2, $SrTiO_3$ and IGZO thin films are shown in Figures 4.9, 4.10 and 4.11, respectively. The binding energies and percentage weights of the existing elements determined to exist on thin films as a result of XPS analysis are shown in detail in Tables 4.2, 4.3 and 4.4. Figure 4.9a, 4.10a and 4.11a show the survey spectrums of HfO_2, $SrTiO_3$ and IGZO thin films, respectively. When XPS high resulation scaning data for HfO_2, $SrTiO_3$ and IGZO are investigated, concerning elements of the peaks that is existing in these thin films were determined as follows.

- The photoelectron peaks of HfO_2 were seen at binding energy of 18.57 eV for the Hf4f and 531.71 eV for the O1s.
- The photoelectron peaks of $SrTiO_3$ were seen at binding energy of 136.60 eV for the Sr3d, 460.97 eV for the Ti2p and 532.47 eV for the O1s.
- The photoelectron peaks of IGZO were seen at binding energy of 1022.05 eV for the Zn2p3, 1118.02 eV for the Ga2p3, 445.16 eV for the In3d5 and 530.79 eV for the O1s.

As a result of the survey scans, it is estimated that C1s elements observed in all thin films are derived from the incidental hydrocarbon from the XPS device itself or from external pollutants, and these carbon peaks and values were neglected in the calculations. The peak positions obtained as a result of XPS analysis of the elements belonging to the materials used in thin film production are in accordance with the values reported in the literature (Khim et al., 2017; Lee et al., 2010; Liang et al., 2010; Ozer et al., 2022).

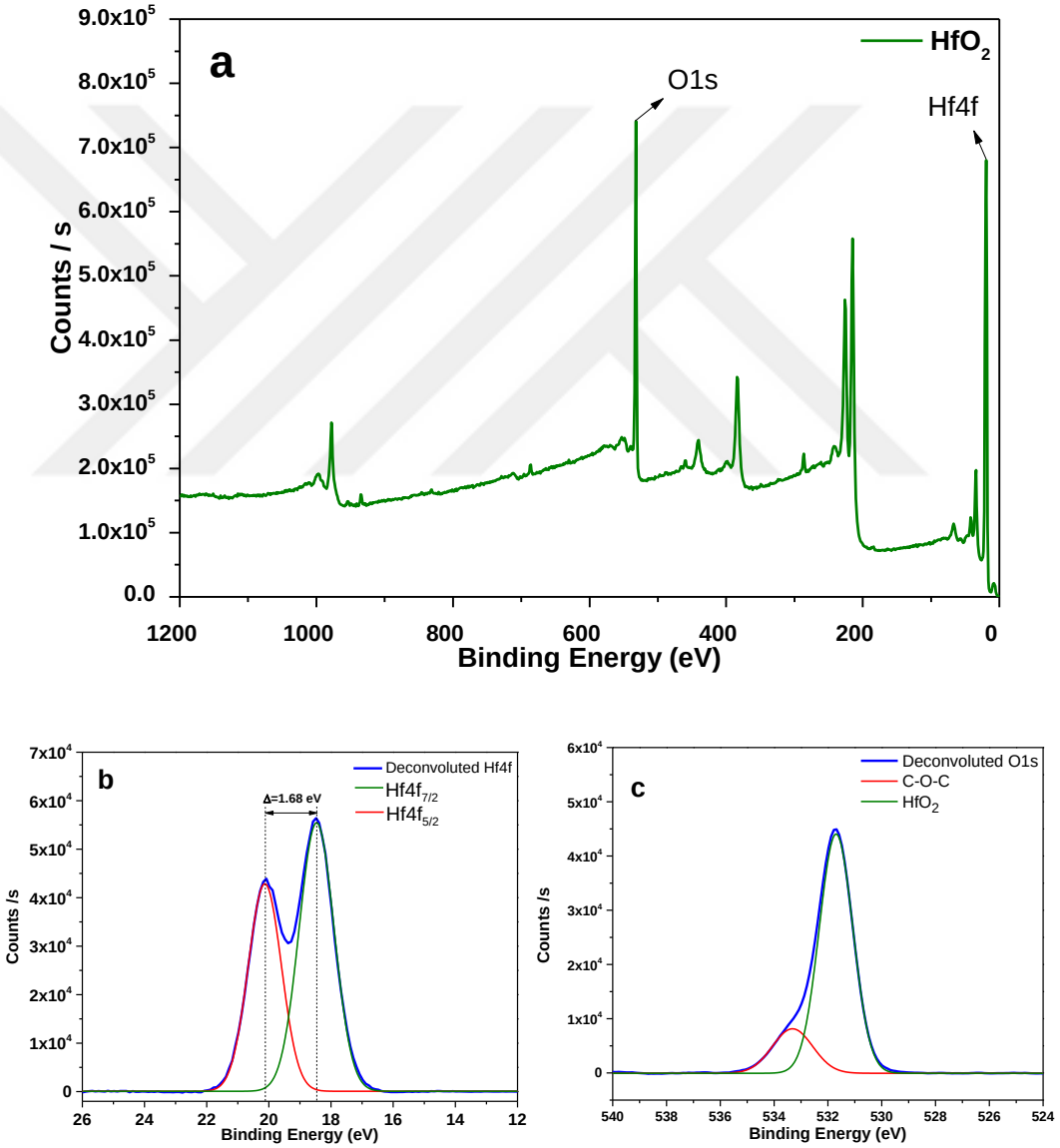


Figure 4.9 XPS spectra of HfO_2 thin film a) survey spectrum, b) deconvoluted Hf4f, c) deconvoluted O1s

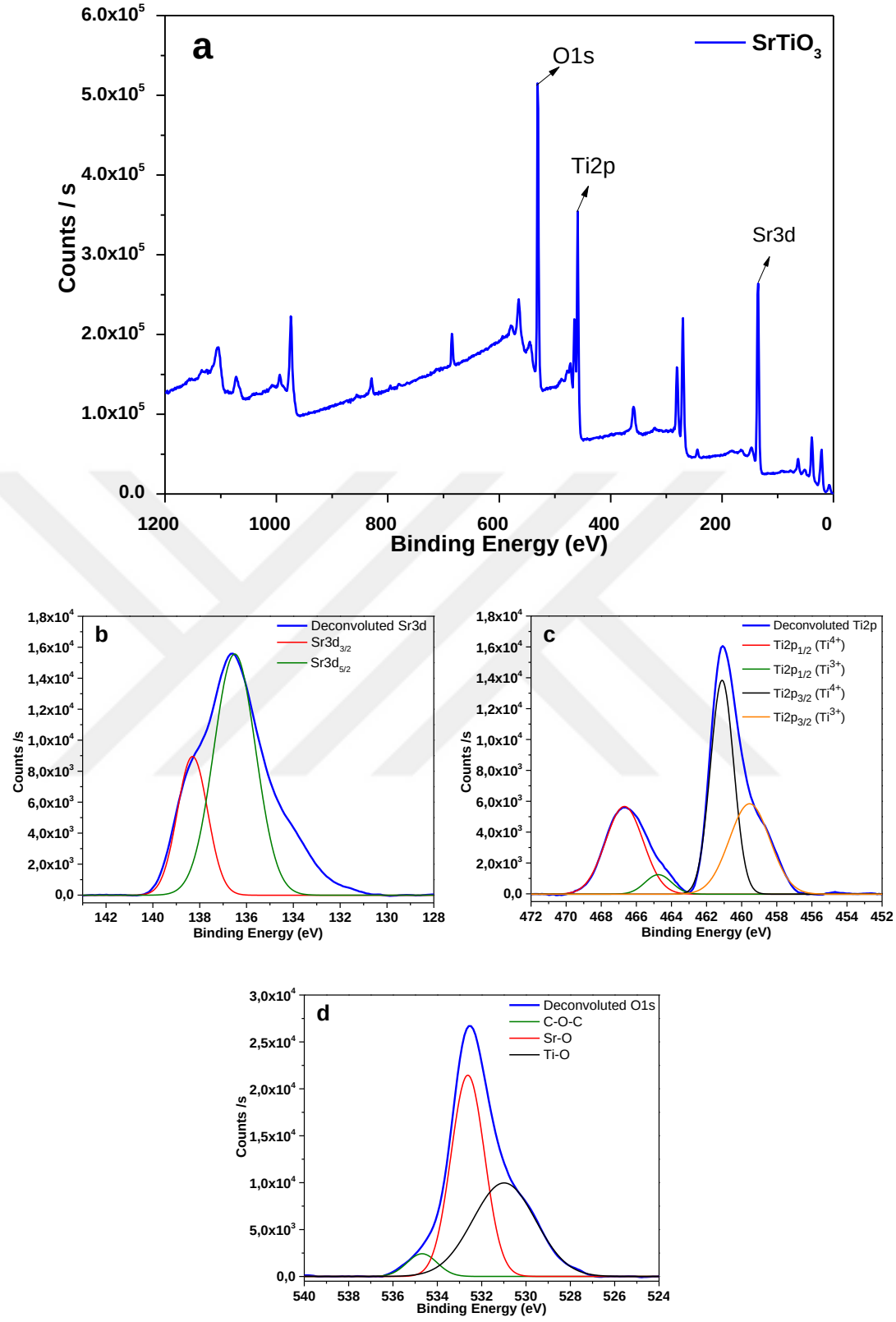


Figure 4.10 XPS data of $SrTiO_3$ thin film a) survey spectrum, b) deconvoluted Sr3d, c) deconvoluted Ti2p, d) deconvoluted O1s

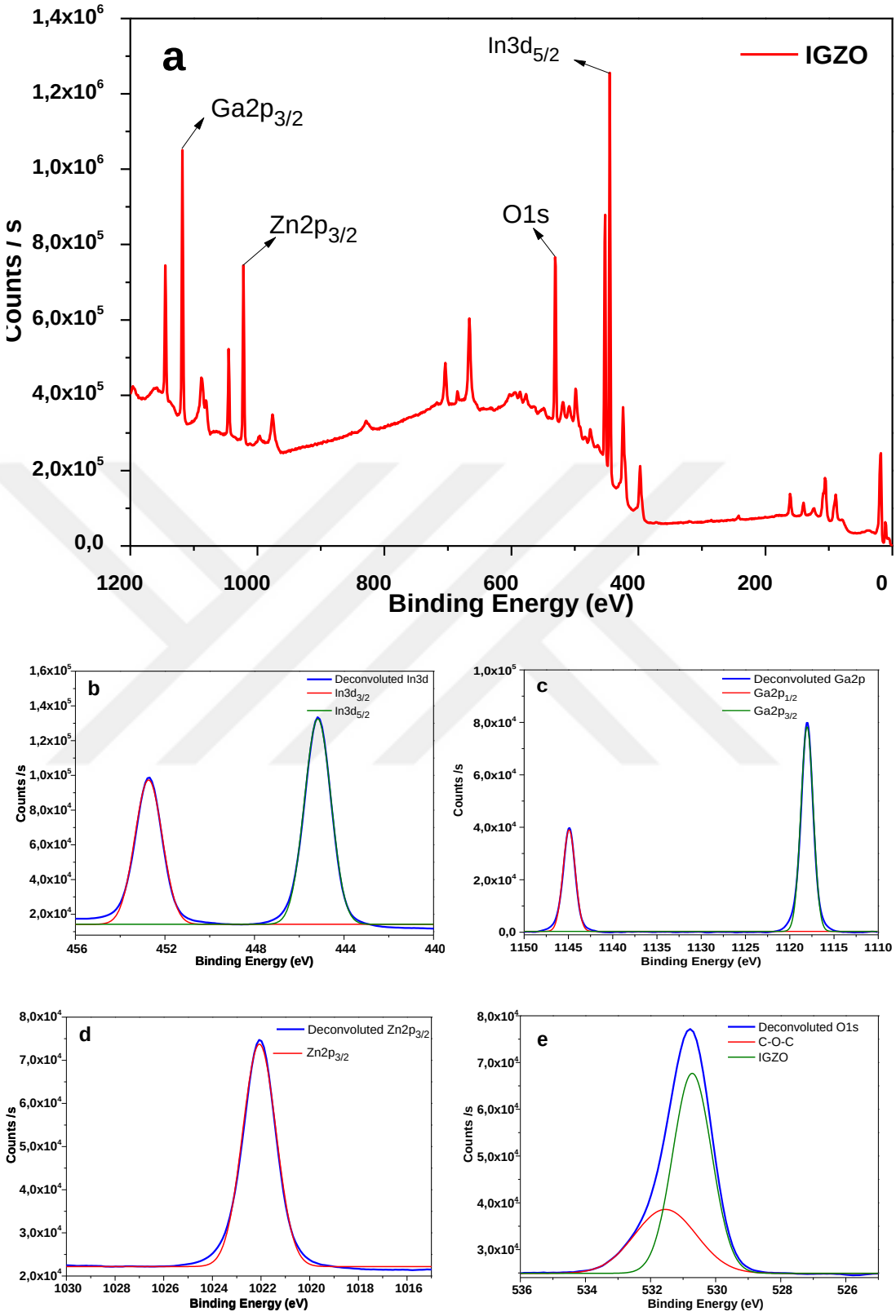


Figure 4.11 XPS data of IGZO thin film a) survey spectrum, b) deconvoluted In3d, c) deconvoluted Ga2p, d) deconvoluted Zn2p3/2, e deconvoluted O1s

Table 4.2 Binding energy and % weight of HfO_2 from XPS data

Name	Start BE	Peak BE	End BE	Weight %
Hf4f	25.68	18.57	13.08	82.47
O1s	536.28	531.71	524.48	17.53

Table 4.3 Binding energy and % weight of $SrTiO_3$ from XPS data

Name	Start BE	Peak BE	End BE	Weight %
Sr3d	141.18	136.6	123.08	36.79
Ti2p	469.98	460.97	449.98	33.61
O1s	536.58	532.47	520.08	29.61

Table 4.4 Binding energy and % weight of IGZO from XPS data

Name	Start BE	Peak BE	End BE	Weight %
Zn2p3	1027.78	1022.05	1014.48	16.36
Ga2p3	1122.68	1118.02	1110.08	29.68
In3d5	448.68	445.16	435.38	35.90
O1s	536.08	530.79	525.88	18.06

When the weight percent values in Tables 4.2, 4.3 and 4.4 are examined, it is seen that HfO_2, $SrTiO_3$ and IGZO thin films can be fabricated in the correct stoichiometry. When XRD and XPS results are evaluated together, it is clearly seen that HfO_2, $SrTiO_3$ and IGZO thin films by production parameters determined for sputtering method can be produced in amorphous and correct stoichiometric structure (Ozer et al., 2022).

In order to improve the electrical performance of the relevant TFT structures, the surface of the HfO_2 gate dielectric layer was coated with $SrTiO_3$ being 2nm, 4nm and 6nm thicknesses respectively, and the interface between the gate dielectric layer and the semiconductor layer in the relevant TFT structures was modified.

As is known, in TFT structures, electrons move at the interface between the semiconductor layer and the dielectric layer. In this region, elements such as oxygen that do not bond with any atom can attract electrons to themselves and cause the electrons to be trapped in this region. In this case, it leads to a decrease in the electrical performance of the respective TFT device, such as the FET mobility value. In TFT structures where oxide semiconductor materials such as IGZO are used, the amount of oxygen to bond with metal atoms at the interface is related to the electronegativity of the metal atoms in this region. In 2017, a similar method has been studied by Kang et al. Kang et al used TaOx as buffer layer between SiO_2 and IGZO to improve the SiO_2 - IGZO semiconductor interface. The electronegativity value of Ta atoms is higher than that of Si atoms. In the TFT structure that surface is modified with TaOx, the number of O atoms bonding with metal atoms at the interface is higher than the one that surface is not modified with TaOx. Thus, after surface modification with TaO, the number of electrons trapped at the interface of the relevant TFT structure was reduced, and therefore the electrical performance of the same TFT device was increased (Kang et al., 2017).

In this study, HfO_2 was used as gate dielectric layer of TFT device and $SrTiO_3$ was used for interface modification. Electronegativity of Ti atom in $SrTiO_3$ is higher than Hf. Thus, after surface modification with $SrTiO_3$, it is planned to reduce the number of oxygen atoms that do not bond with metal atoms at the interface before the modification.

Considering the layer thickness of the produced TFT structures, elemental XPS analysis was performed at 5nm, 15nm and 25nm depths, respectively, in order to find the percentage of bonding of the oxygen atom with metal atoms between the dielectric layer and the semiconductor layer of the relevant TFT devices (See fig 4.12, 4.13 and 4.14).

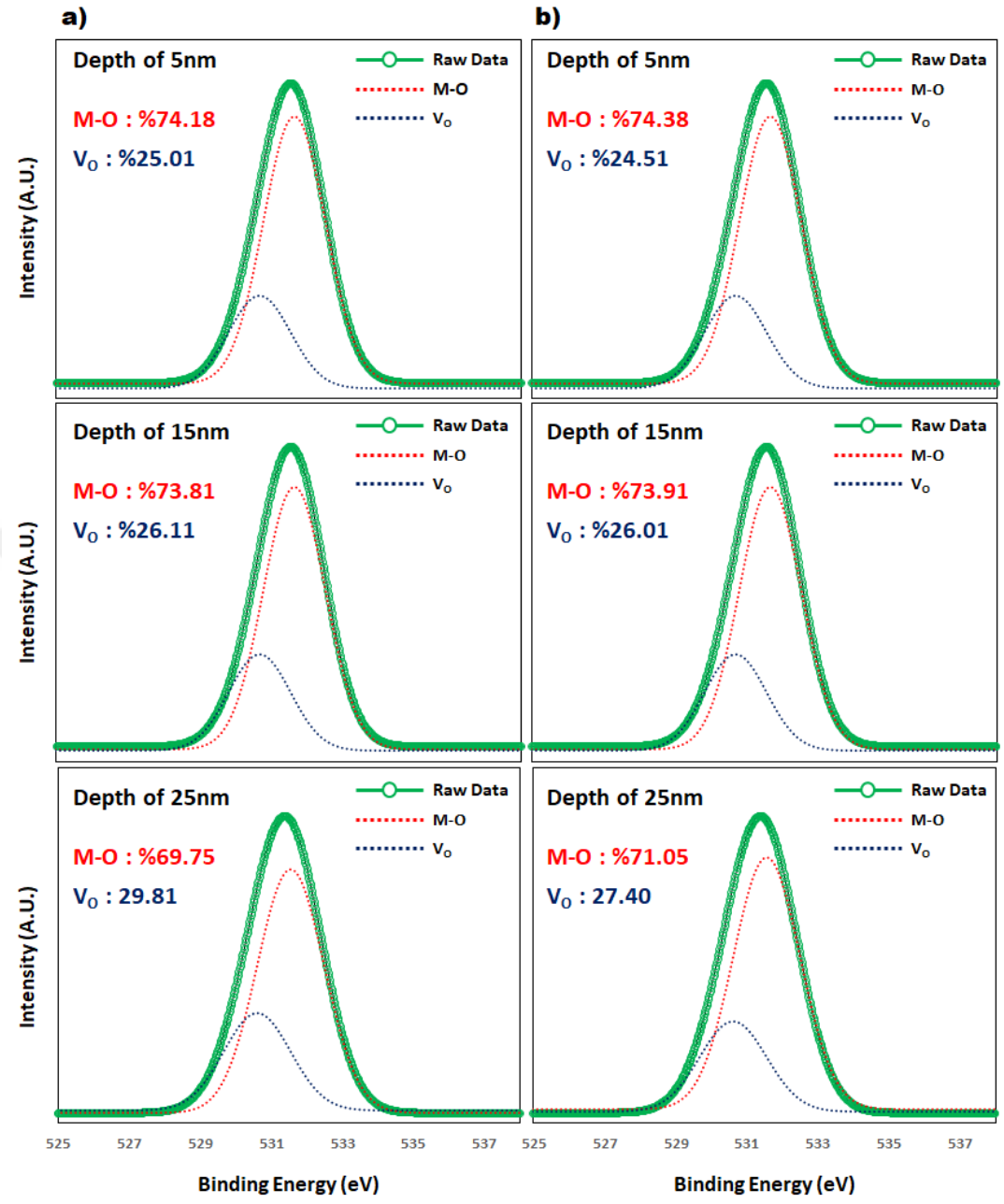


Figure 4.12 Change of Metal-Oxygen bond amount depending on depth in HfO_2 vs HfO_2 + 2nm $SrTiO_3$ structures

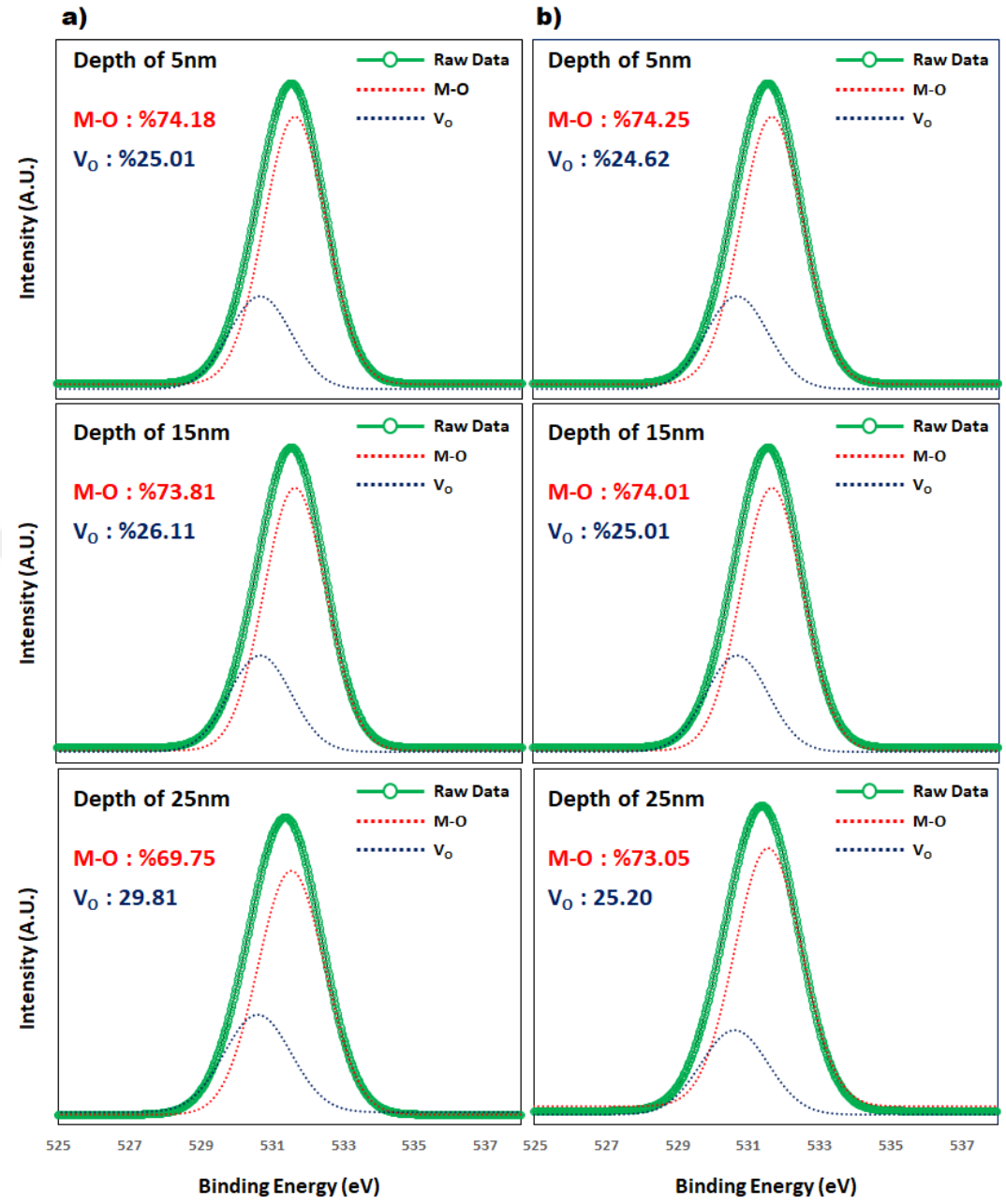


Figure 4.13 Change of Metal-Oxygen bond amount depending on depth in HfO_2 vs HfO_2 + 4nm $SrTiO_3$ structures

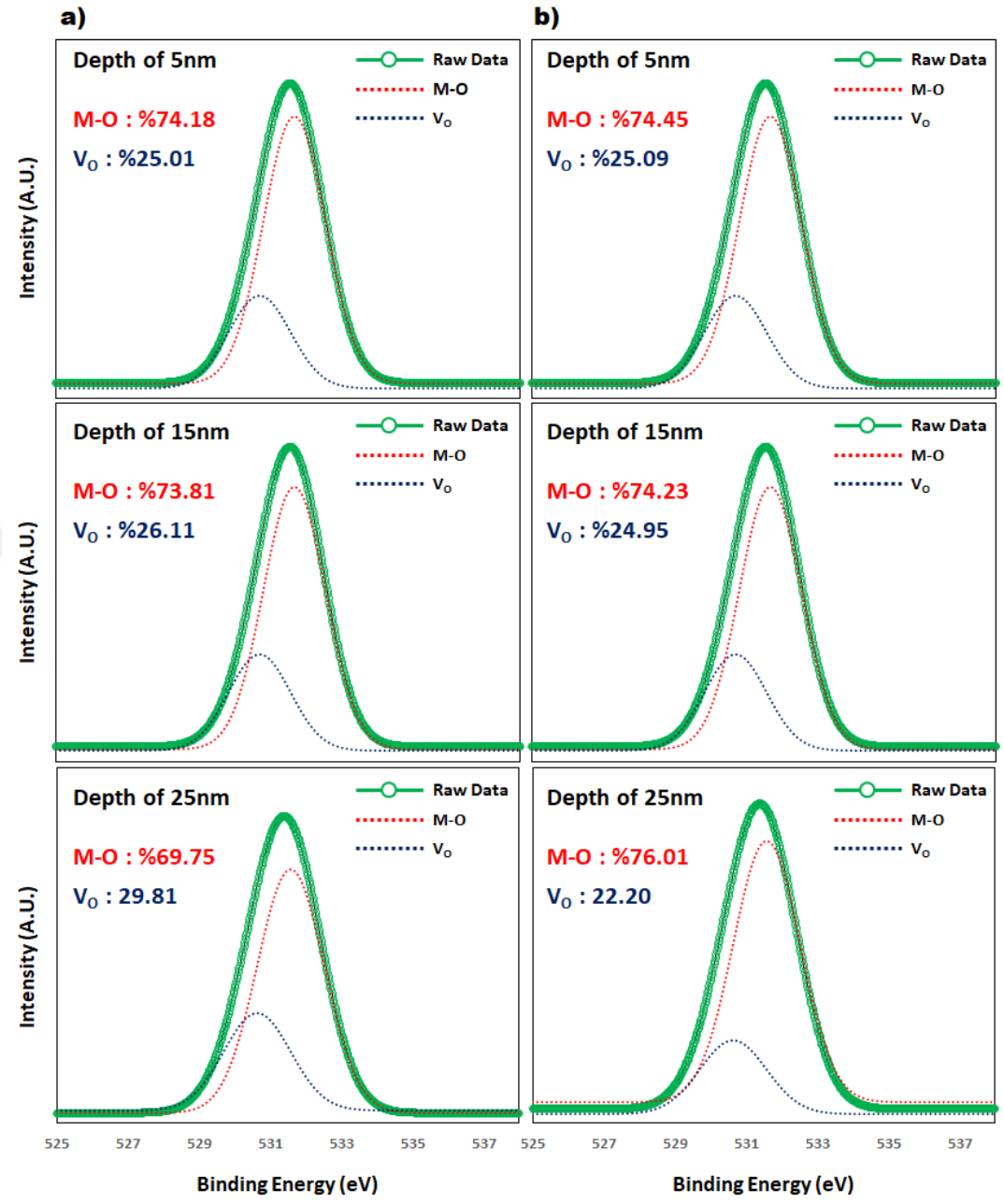


Figure 4.14 Change of Metal-Oxygen bond amount depending on depth in HfO_2 vs HfO_2 + 6nm $SrTiO_3$ structures

The graphs shown in Figures 4.12a, 4.13a and 4.14a are the results of the XPS depth analysis of the TFT device that surface has not been modified and it has been used for comparison with the surface modified structure. When the results in Figures 4.12b, 4.13b and 4.14b are examined, it is clearly seen that the number of oxygen atoms bonded with metal atoms increases with the increasing $SrTiO_3$ thickness according to the measurements made at the 25nm depth corresponding to the interface. The results of the XPS depth analysis clearly show that the probability of trapping electrons at the interface will be reduced by the surface modification process.

4.1.4 AFM Analysis

The surface mophologies of each of the HfO_2 and $SrTiO_3$ thin films produced for the calibration of the sputter system with a thickness of approximately 50nm are shown in Figure 4.15. In addition, the surface roughness values of the relevant thin films are shared in Table 4.5 and Figure 4.16.

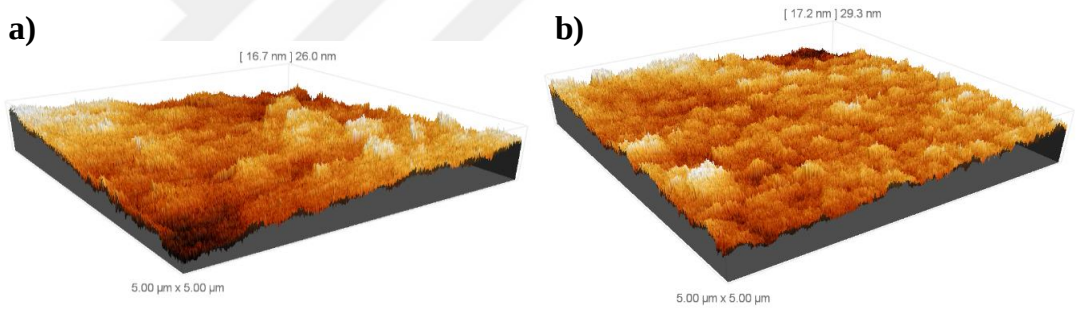


Figure 4.15 AFM results a) 50nm HfO_2 and b) 50nm $SrTiO_3$ thin films

Table 4.5 Average roughness values of HfO_2 and $SrTiO_3$ thin films having 50nm thickness

Sample Layers	**Scan Area (m x m)**	**Peak-Peak Height (nm)**	**Average Roughness (nm)**
HfO_2: 56.74nm	5 x 5	19.1	1.5
$SrTiO_3$: 55.43nm	5 x 5	19.2	1.5

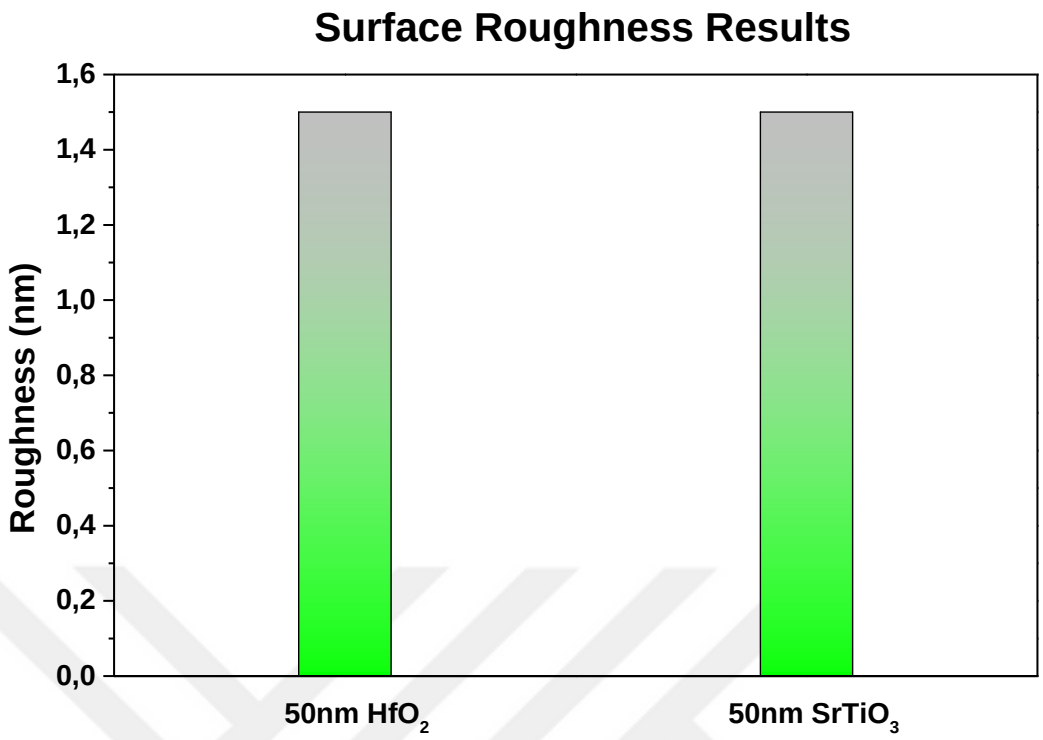


Figure 4.16 Average roughness values of HfO_2 and $SrTiO_3$ thin films

AFM results showed that HfO_2 and $SrTiO_3$ thin films being TFT's gate dielectric and buffer layer can be produced with a surface roughness of 1.5nm. This value clearly shows that the relevant layers can be produced with low surface roughness by sputtering method for flexible transparent TFT application. On the other hand, when TFT applications in the literature are examined, it is seen that the surface roughness values of TFT devices with good electrical performance are almost the same or worse than the flexible transparent TFT structure developed in this study (Aoki & Kunitake, 2004; Han et al., 2018; Lee, Jeong, et al., 2017; Park et al., 2009).

AFM analysis results of HfO_2 and HfO_2+$SrTiO_3$ thin films produced with sputtering production parameters verified according to XRD and XPS results are shown in Figure 4.17. Thickness of regarding thin films are shared in Figure 4.17. In addition, the surface roughness values of the relevant thin films are shown in table 4.6 and Figure 4.18.

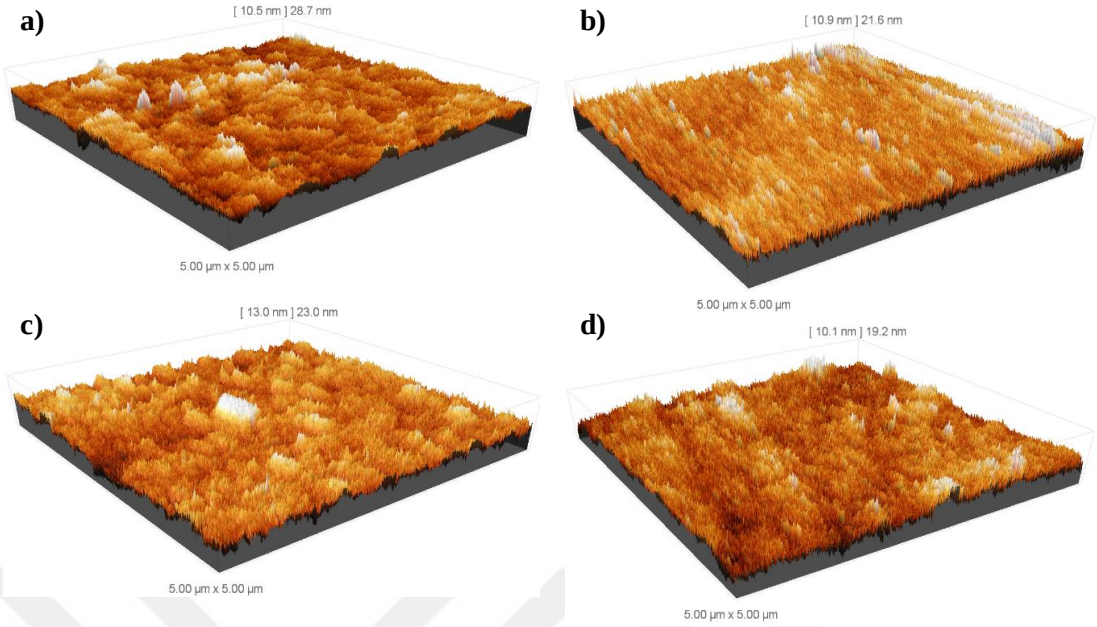


Figure 4.17 AFM results a) 40nm HfO_2, b) 40nm HfO_2 + 2nmSr TiO_3, c) 40nm HfO_2 + 4 nmSr TiO_3 and d) 40nm HfO_2 + 6nmSr TiO_3 thin films

Table 4.6 Average roughness values of HfO_2+$SrTiO_3$ thin films having below thicknesses

Sample Layers	**Scan Area (m x m)**	**Peak-Peak Height (nm)**	**Average Roughness (nm)**
HfO_2: 40nm	5 x 5	10.5	1.5
HfO_2: 40nm + $SrTiO_3$: 2nm	5 x 5	10.9	1.4
HfO_2: 40nm + $SrTiO_3$: 4nm	5 x 5	13.0	1.5
HfO_2: 40nm + $SrTiO_3$: 6nm	5 x 5	10.1	1.7

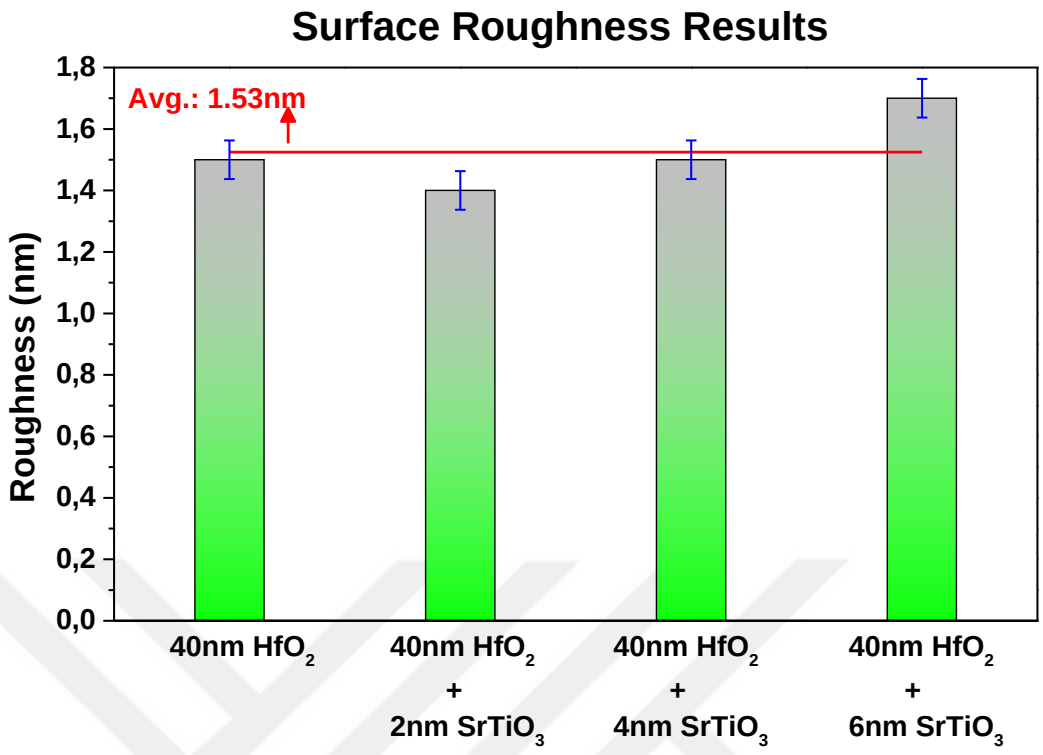


Figure 4.18 Average roughness values of HfO_2+$SrTiO_3$ thin films

AFM results showed that HfO_2 and HfO_2+$SrTiO_3$ thin films being TFT's gate dielectric and buffer layer can be produced with a surface roughness of approximately 1.5nm. This value clearly shows that the relevant layers were produced with low surface roughness by sputtering method for flexible transparent TFT in this study.

The roughness of the surface of the dielectric structure on which the semiconductor layer will be formed is very important. Because in TFTs, electrons move at this interface between the semiconductor layer and the dielectric layer. If the surface roughness of this dielectric layer is high, this causes the movement of electrons at the interface to be difficult and the electrical performance of the relevant TFT structure to decrease.

The single and dual dielectric structure produced in this study has a good surface roughness that does not cause any deterioration in the electrical performance of the relevant TFT structure when compared with the dielectric structures in the literature (Aoki & Kunitake, 2004; Han et al., 2018; Lee, Jeong, et al., 2017; Park et al., 2009).

4.1.5 Optical Transparency Results of Flexible Transparent TFTs

In Figure 4.19, optical transmittance spectra of related TFT devices with shared layer thicknesses are shown.

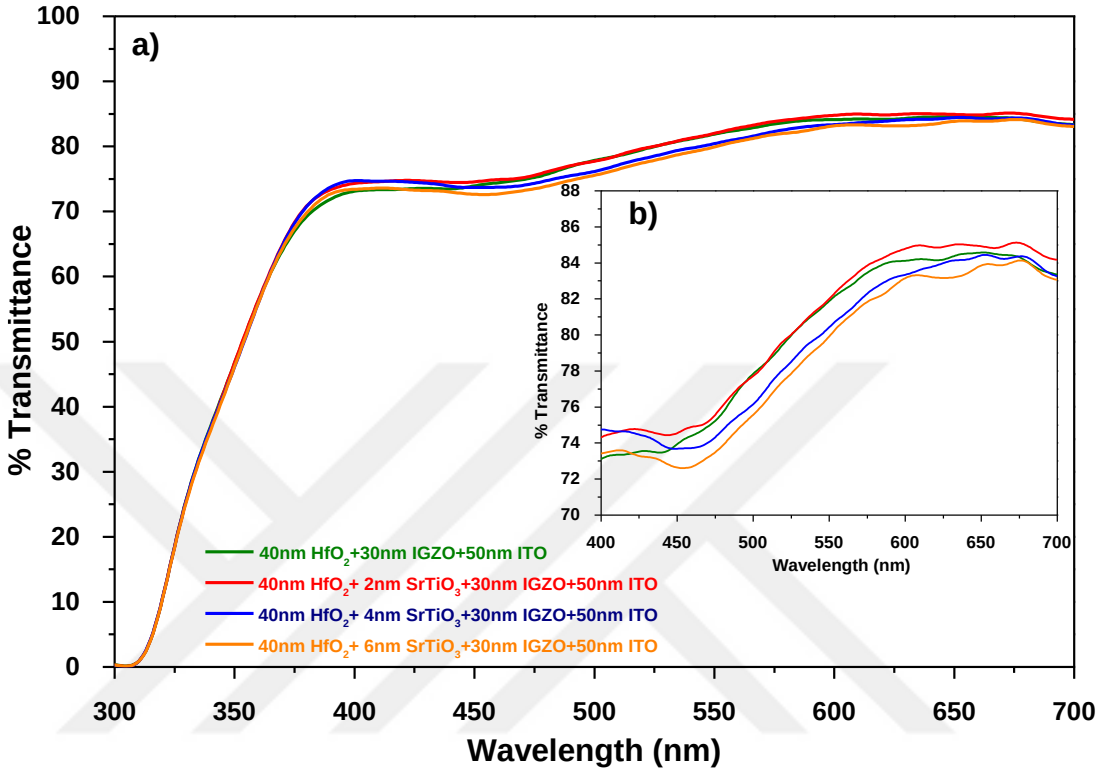


Figure 4.19 Optical transmittance spectrums for flexible transparent TFTs a) wavelength range from 300nm to 700nm b) wavelength range from 400nm to 700nm (for visible region)

The results in Figure 4.19b, 4.20 and Table 4.7 clearly show that the optical transmittance values of the produced flexible transparent TFTs in this study are average 79% between 400-700nm.

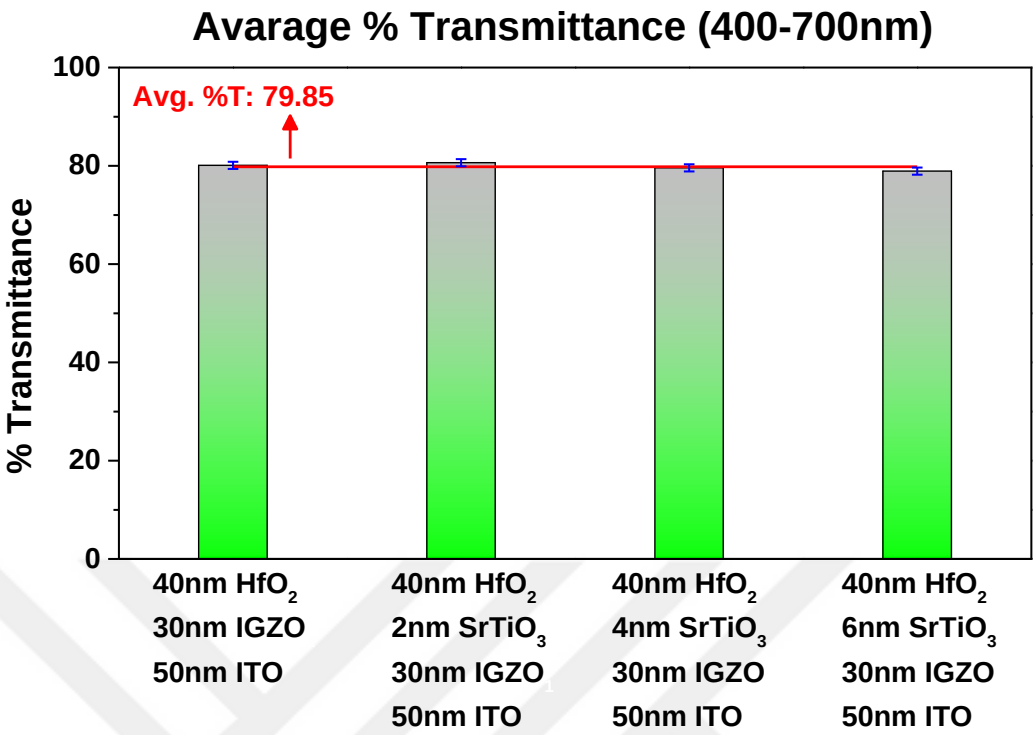


Figure 4.20 Avarage %transmittance values for related TFT structures

Table 4.7 Avarage %transmittance values of concerning TFT devices for visible region of electromagnetic spectrum

Layers and Thicknesses	**Avg. %Transmittance (400-700nm)**	**%T Avg.**
40nm HfO_2+30nm IGZO+50nm ITO	80.09	79.80
40nm HfO_2+2nm $SrTiO_3$+30nm IGZO+50nm ITO	80.63	79.80
40nm HfO_2+4nm $SrTiO_3$+30nm IGZO+50nm ITO	79.58	79.80
40nm HfO_2+6nm $SrTiO_3$+30nm IGZO+50nm ITO	78.92	79.80

According to these results, it is clearly seen that the optical transmittance value of the developed flexible transparent TFT (Ozer et al., 2022) is at an appropriate or much better level compared to the studies in the literature (Fan et al., 2019; Hsieh et al., 2010; Mativenga et al., 2015; Rembert et al., 2015).

4.2 Results of Electrical Characterizations for TFTs

After the thickness calibration of the sputter system, the layer and contact thicknesses of the TFT structures developed with the relevant fabrication parameters are shown in Table 4.8. In order to see the effect of different channel geometries, the relevant flexible transparent TFT structure has been fabricated in the same layer thickness. With the help of the special shadow mask used, the channel geometries of this TFT structure with the same layer thicknesses were adjusted as indicated in Table 4.8.

Table 4.8 Active channel geometries for HfO_2+IGZO TFT structures

TFTs	HfO_2 Thickness (nm)	IGZO Thickness (nm)	ITO Thickness (nm)	Channel Width (µm)	Channel Lenght (µm)
Device1	40	30	50	1000	80
Device2	40	30	50	1000	60
Device3	40	30	50	1000	50
Device4	40	30	50	1000	40
Device5	40	30	50	1000	30

In this structure that is shown in Table 4.8, gate dielectric layer, semiconductor layer and Source-drain contacts of TFT strucute consist of HfO~~2~~, IGZO and ITO materials, respectively. The graphics about transfer characteristics of the respective TFT devices are shown in Figure 4.21. For this measurements, V_{ds} voltage of the corresponding TFT structure setted as 2.5V. V_{gs} voltage was sweepted from 0V to 5V. I_{ds} currents data corresponding to the V_{gs} voltages at these measurement conditions were collected. In order to calculate μ_{FET} and V_{th} parameters, the graph in Figure 4.21b was obtained by taking the square root of I_{ds} current values.

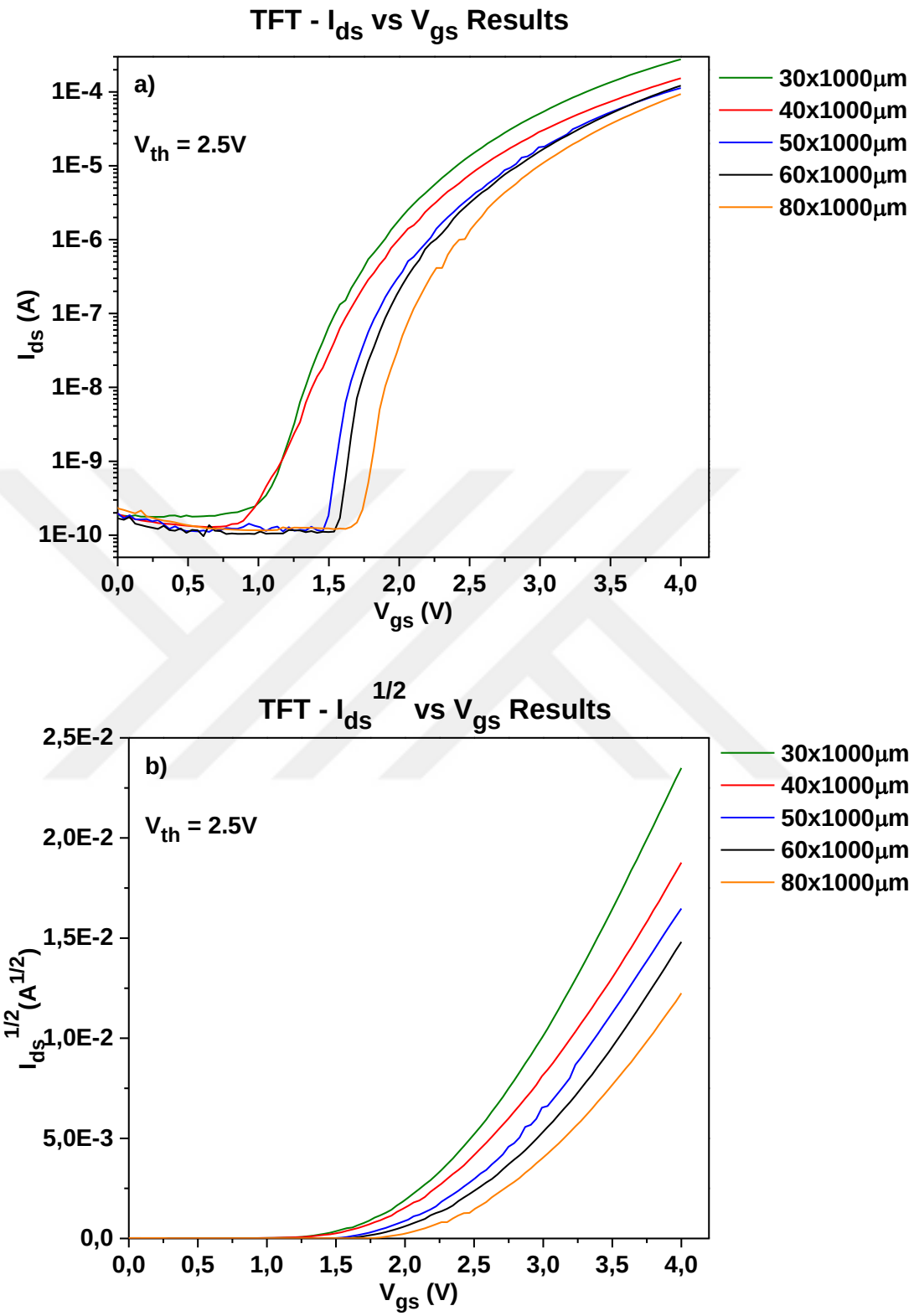


Figure 4.21 Transfer characteristics of HfO_2+IGZO TFT a) I_{ds} vs V_{gs} plots and b) $I_{ds}^{1/2}$ vs V_{gs} plots

The graph and data in Figure 4.21 were created by applying the linner curve fitting method to the relevant parts of the data in Figure 4.20b. Using the data in Figure 4.20a and Figure 4.21, μ_{FET}, V_{th}, Source-Drain leakage current ($I_{ds\text{-}leakage}$) and Ion/Off ratio values shared in Table 4.9 were calculated for the relevant TFT structures.

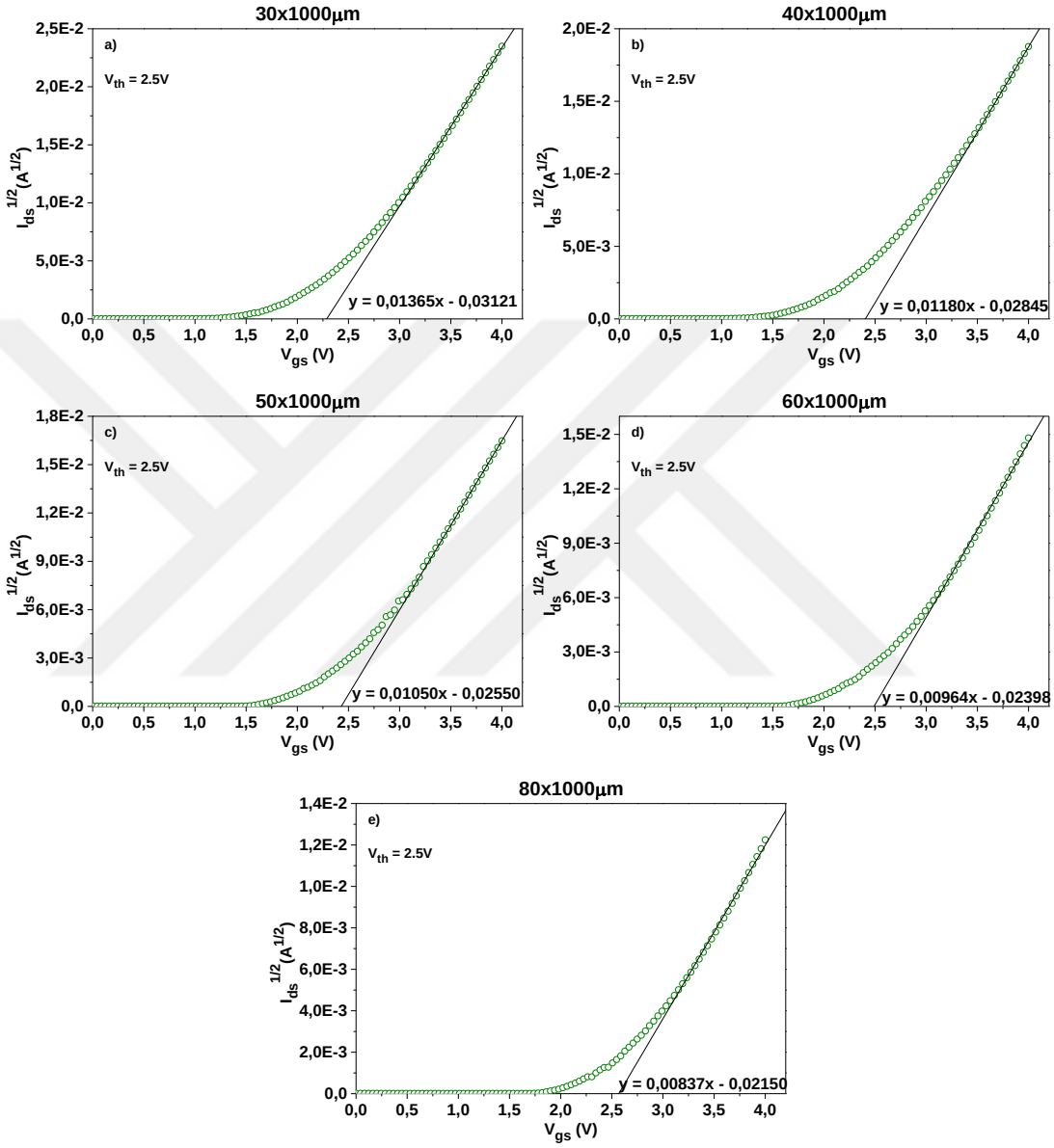


Figure 4.22 Curve fitted transfer characteristics of HfO_2+IGZO TFT structure with different channel geometries a) W=1000µm and L=30µm, b) W=1000µm and L=40µm, c) W=1000µm and L=50µm, d) W=1000µm and L=60µm and e) W=1000µm and L=80µm

Table 4.9 μ_{FET}, V_{th}, $I_{ds\text{-}leakage}$ and $I_{on}/_{Off}$ ratio of HfO_2+IGZO TFT structure

TFT Channel Geometry	W (cm)	L (cm)	μ_{FET} (cm^2/Vs)	V_{th} (V)	$I_{ds\text{-}leakage}$ (A)	I_{on}/I_{off}
80x1000µm	0.1	0.008	20.27	2.57	$1.18x10^{-10}$	$8.10x10^{5}$
60x1000µm	0.1	0.006	20.16	2.49	$1.03x10^{-10}$	$1.26x10^{6}$
50x1000µm	0.1	0.005	19.93	2.43	$1.25x10^{-10}$	$1.02x10^{6}$
40x1000µm	0.1	0.004	20.14	2.41	$1.32x10^{-10}$	$1.20x10^{6}$
30x1000µm	0.1	0.003	20.21	2.29	$1.80x10^{-10}$	$1.57x10^{6}$

According to the calculations in Table 4.9, the average fet mobility value of the relevant flexible transparent TFT structures is calculated as 20.14 cm^2/Vs. In addition, it is seen that the V_{th} value varies between 2.29V and 2.57V and the I_{on}/I_{off} ratio value varies between $8.10x10^5$ and $1.57x10^6$. It is thought that the variation in V_{th} and I_{on}/I_{off} ratio values is due to the deviation of the thickness of the dielectric and semiconductor layers from the values that should be after production. However, when the TFT structure developed in this study is compared with its counterparts in the literature, it is clearly seen that μ_{FET}, V_{th} and I_{on}/I_{off} values of this TFT device are at a very good level (Itagaki et al., 2008; Jang et al., 2015; Khim et al., 2017; Ko et al., 2011; Rudenja et al., 2010).

It is known that the maximum current that can flow through the active channel is related to the channel geometry. In this context, the results obtained correspond exactly to this finding. However, due to the special shadow mask used in TFT fabrication, the production repeatability of the structure with the longest channel geometry is more reliable. Therefore, the effects of the interface modification have been investigated on the TFT device with the largest channel geometry that channel length is 80 µm. Thus, production-related errors have been reduced to a negligible level.

The channel geometries, layer thicknesses and device codes of the TFT devices preferred for this purpose are given in Table 4.10.

Table 4.10 Preferred TFT structure to verify production repeatability

Device Code	Channel Width (µm)	Channel Length (µm)	HfO2 Thickness (nm)	IGZO Thickness (nm)	ITO Thickness (nm)
TFT1	1000	80	40	30	50
TFT2	1000	80	40	30	50
TFT3	1000	80	40	30	50
TFT4	1000	80	40	30	50

Figure 4.23 shows the transfer characteristics of the relevant TFT devices and also, Figure 4.24 shows μ_{FET}, V_{th}, $I_{ds\text{-}leakage}$ and I_{on}/I_{off} ratio values of the same TFT devices.

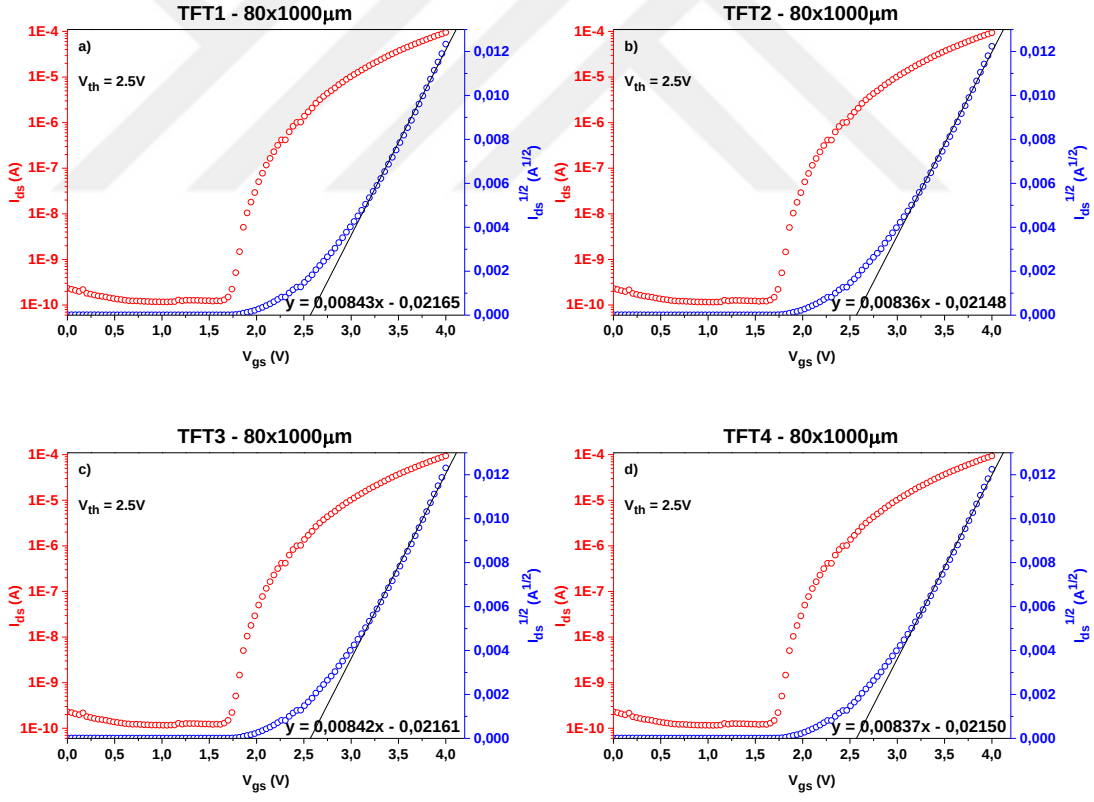


Figure 4.23 Transfer characteristics of concerning TFT devices a) for TFT1, b) for TFT2, c) for TFT3 and d) for TFT4

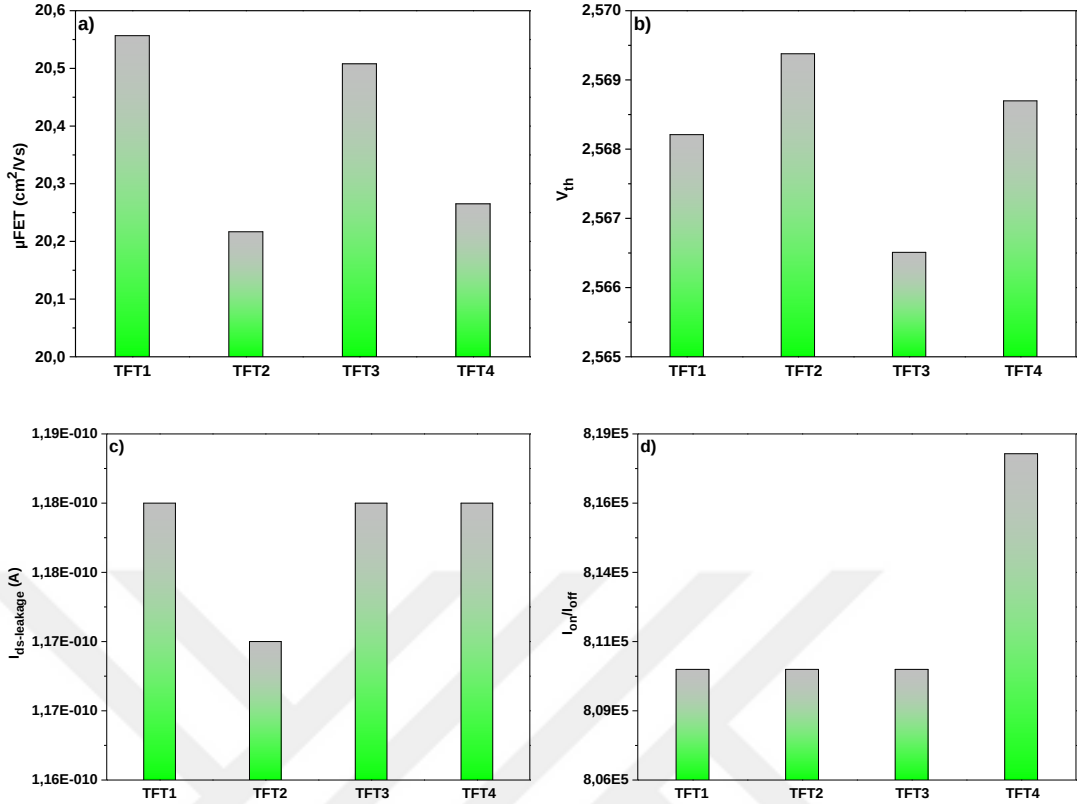


Figure 4.24 Electrical parameters of TFT1, TFT2, TFT3 and TFT4 devices a) μ_{FET} values, b) V_{th} values, c) $I_{ds\text{-}leakage}$ values and d) I_{on}/I_{off} ratios

Table 4.11 Electrical parameters and avarage values of concerning TFT devices

TFTs	**μ_{FET} (cm^2/Vs)**	**V_{th} (V)**	**$I_{ds\text{-}leakage}$ (A)**	**I_{on}/I_{off}**
TFT1	20.56	2.57	$1.18x10^{-10}$	$8.10x10^{5}$
TFT2	20.22	2.57	$1.17x10^{-10}$	$8.10x10^{5}$
TFT3	20.51	2.57	$1.18x10^{-10}$	$8.10x10^{5}$
TFT4	20.27	2.57	$1.18x10^{-10}$	$8.18x10^{5}$
Avarage Values	**20.39**	**2.57**	**$1.18x10^{-10}$**	**$8.12x10^{5}$**

The results in Table 4.11 can be regarded as the same for the TFT device with the corresponding channel geometry. This shows that the reproducibility of the TFT device with the relevant channel geometry is very high and the production-related error formation is very low.

After determining the appropriate channel geometry for the TFT structure to be modified as explained above, the layer and Source-Drain contacts thicknesses of the

TFT structures developed with the relevant fabrication parameters are shown in Table 4.12. In order to see the effect of different $SrTiO_3$ thicknesses as a buffer layer of TFT device, the relevant flexible transparent TFT structure has been fabricated in the same channel geometry with different $SrTiO_3$ thickness that is shown in table 4.12. With the help of the special shadow mask used, the channel geometries of these TFT structures with the different $SrTiO_3$ layer thicknesses were adjusted as indicated in Table 4.12.

Table 4.12 TFT device configuration for HfO_2+$SrTiO_3$+IGZO TFT structures

TFTs	**HfO2 Thickness (nm)**	**$SrTiO_3$ Thickness (nm)**	**IGZO Thickness (nm)**	**ITO Thickness (nm)**	**Channel Width (µm)**	**Channel Lenght (µm)**
TFT-S1	40	0	30	50	1000	80
TFT-S2	40	2	30	50	1000	80
TFT-S3	40	4	30	50	1000	80
TFT-S4	40	6	30	50	1000	80

In these structures that is shown in Table 4.12, gate dielectric layer, buffer layer, semiconductor layer and Source-Drain contacts of TFT strucutes consist of HfO_2, $SrTiO_3$, IGZO and ITO materials, respectively. The graphics about transfer characteristics of the respective TFT devices are shown in Figure 4.25. For this measurements, V_{ds} voltage of the corresponding TFT structure setted as 2.5V. V_{gs} voltage was sweepted from 0V to 5V. I_{ds} currents data corresponding to the V_{gs} voltages at these measurement conditions were collected. In order to calculate μ_{FET} and V_{th} parameters, the graph in Figure 4.25b was obtained by taking the square root of I_{ds} current values.

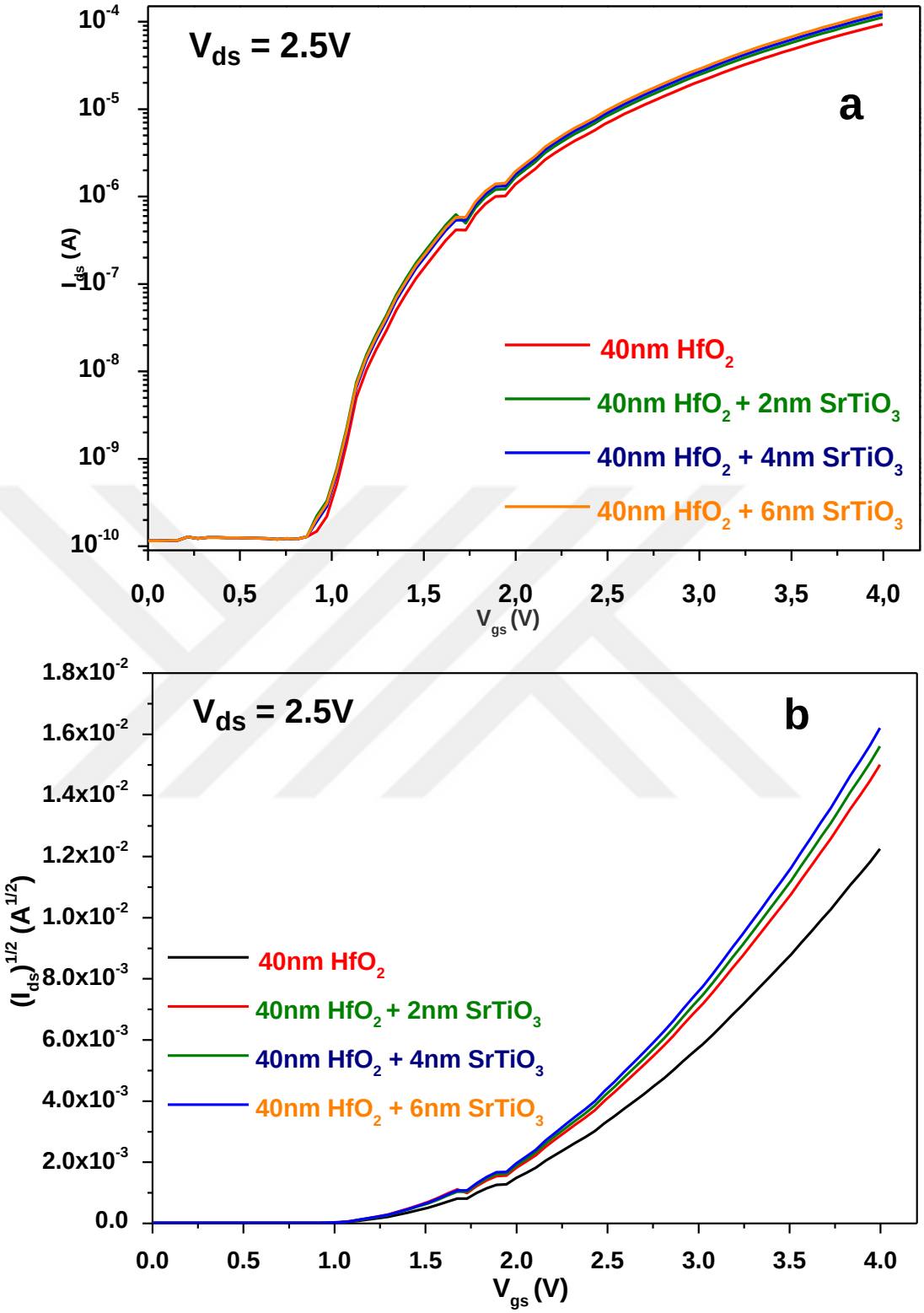


Figure 4.25 Transfer characteristics of HfO_2+IGZO and HfO_2+$SrTiO_3$+IGZO TFTs a) I_{ds} vs V_{gs} plots and b) $I_{ds}^{1/2}$ vs V_{gs} plots

The graph and data in Figure 4.26 were created by applying the linner curve fitting method to the relevant parts of the data in Figure 4.25b. Using the data in Figure 4.25a and Figure 4.26, μ_{FET}, V_{th}, Source-Drain leakage current ($I_{ds\text{-}leakage}$) and I_{on}/I_{off} ratio values shared in Table 4.3 were calculated for the relevant TFT structures.

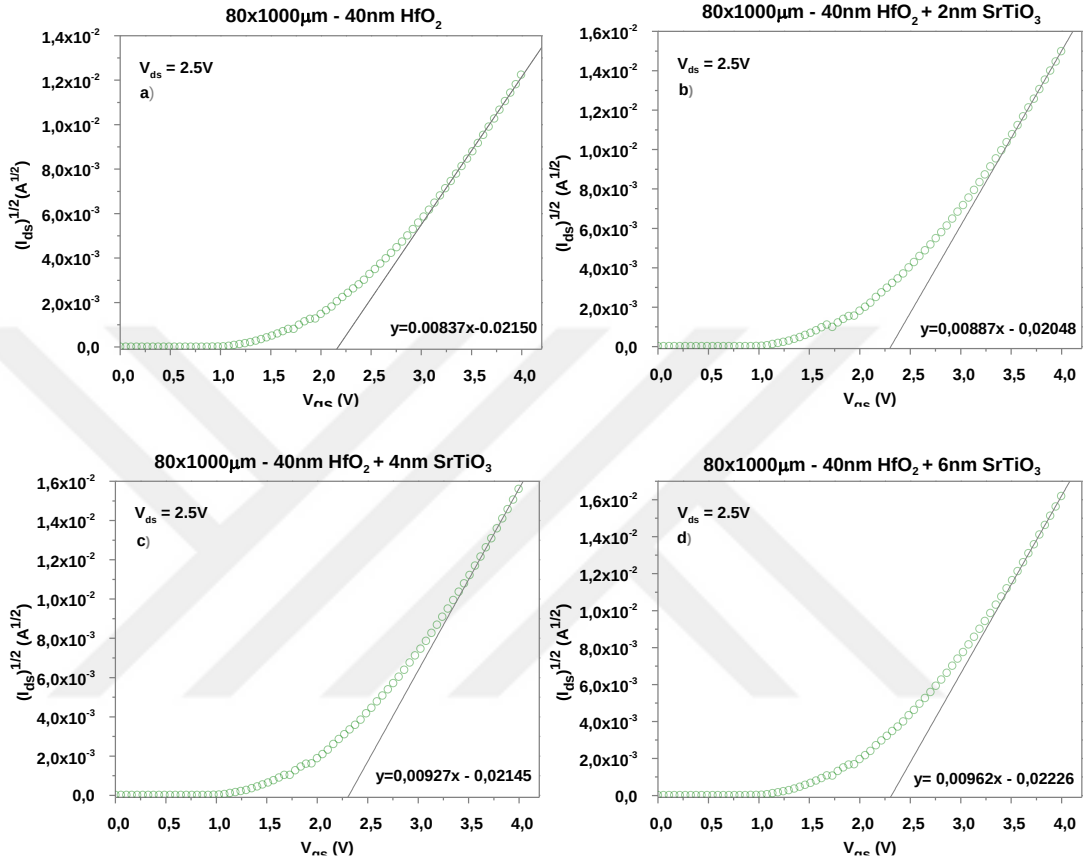


Figure 4.26 Curve fitted transfer characteristics of HfO_2+IGZO and HfO_2+$SrTiO_3$+IGZO TFT structures

Table 4.13 μ_{FET}, V_{th}, $I_{ds\text{-}leakage}$ and I_{on}/I_{Off} ratio of HfO_2+IGZO and HfO_2+$SrTiO_3$+IGZO TFT structures

TFT Device Code	W (cm)	L (cm)	μ_{FET} (cm^2/VS)	V_{th} (V)	$I_{ds\text{-}leakage}$ (A)	I_{on}/I_{off}
TFT-S1	0.1	0.008	20.27	2.57	$1.18x10^{-10}$	$8.10x10^{5}$
TFT-S2	0.1	0.008	22.77	2.31	$1.23x10^{-10}$	$9.72x10^{5}$
TFT-S3	0.1	0.008	24.89	2.31	$1.23x10^{-10}$	$1.05x10^{6}$
TFT-S4	0.1	0.008	26.82	2.31	$1.18x10^{-10}$	$1.13x10^{6}$

According to the calculations in Table 4.13, the fet mobility values of the respective TFT devices increase with increasing $SrTiO_3$ buffer layer thickness. The maximum fet mobility value of 26.82 cm^2/Vs was obtained for the TFT device with maximum $SrTiO_3$ thickness that is 6nm (See Table 4.13). When the fet mobility value obtained for this TFT structure is compared with the studies in the literature, it is clearly seen that this fet mobility value obtained for the new generation flexible and transparent TFT device developed with this innovative method is at a very competitive level (Itagaki et al., 2008; Jang et al., 2015; Khim et al., 2017; Ko et al., 2011; Ozer et al., 2022; Rudenja et al., 2010).

As stated in the XPS depth analysis results, with increasing $SrTiO_3$ thickness, the number of metal atoms not bonded with oxygen between the dielectric layer and the semiconductor layer decreases compared to the situation where the $SrTiO_3$ buffer layer is not used. This is because the Sr and Ti atoms have a higher capacity to bond with O than the Hf atom. Thus, easier movement of electrons in the intermediate layer modified with $SrTiO_3$ was provided. For this reason, fet mobility values of the related TFT structures increased compared to the unmodified TFT structure. A similar study was performed by Kang et al in 2017 using TaOx as buffer layer between SiO_2 and IGZO to improve the SiO_2 - IGZO semiconductor interface (Kang et al., 2017).

In addition, the fact that V_{th}, $I_{ds\text{-}leakage}$ and I_{on}/I_{off} values are almost the same in all developed TFT devices shows that there is repeatability in multiple productions for the relevant production method.

The results shared in Figure 4.26 and table 4.13 were obtained before the relevant TFT devices entered the reliability tests. According to these results, the TFT device with the best electrical performance before environmental tests is the "TFT-S4" coded device. This TFT device has been subjected to TCT, TST and HTHH tests, which simulate the important environmental test conditions of products produced for display technologies, and after these tests, the electrical performance of the relevant product has been redetermined.

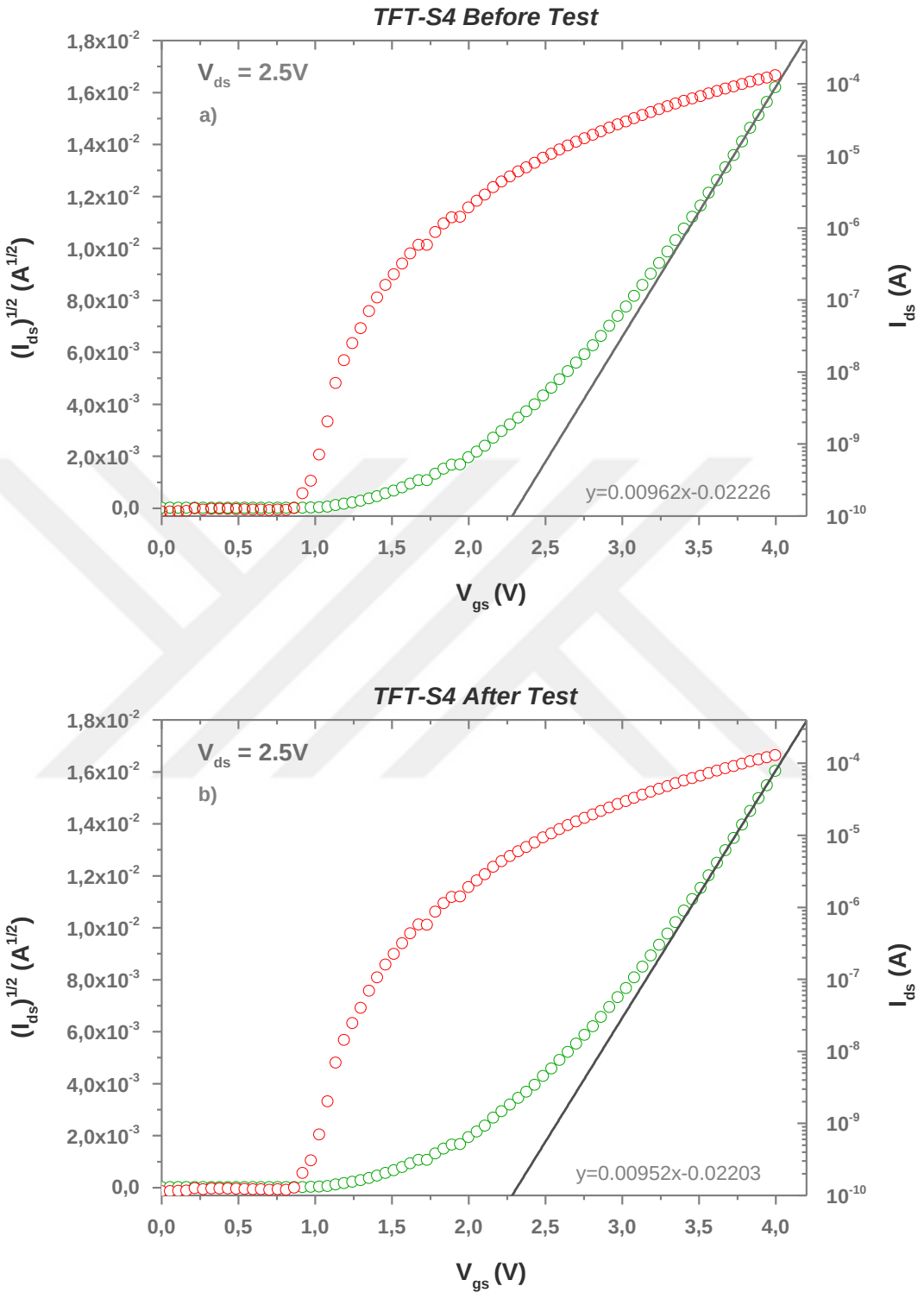


Figure 4.27 Transfer characteristic of the relevant TFT device a) before environmental tests and b) after environmental tests

Table 4.14 μ_{FET}, V_{th}, $I_{ds\text{-}leakage}$ and $I_{on}/_{Off}$ ratio of TFT-S4 device before and after enviromental tests

TFT Device Code	**W (cm)**	**L (cm)**	**μ_{FET} (cm^2/VS)**	**V_{th} (V)**	**$I_{ds\text{-}leakage}$ (A)**	**I_{on}/I_{off}**
TFT-S4 before tests	0.1	0.008	26.82	2.31	$1.18x10^{-10}$	$1.13x10^{6}$
TFT-S4 after tests	0.1	0.008	26.27	2.31	$1.17x10^{-10}$	$1.13x10^{6}$

According to the results of the measurements made before and after the TCT, TST and HTHH tests, shown in Figure 4.27 and Table 4.14, the fet mobility value of the relevant TFT device before the test was 26.82 cm^2/Vs, while it decreased to 26.27 cm^2/Vs after the tests. However, there was no change in V_{th}, $I_{ds\text{-}leakage}$ and I_{on}/I_{off} values of the relevant TFT after the reliability tests.

The fact that there is no significant change in the electrical performance of the relevant TFT device after the TCT, TST and HTHH tests, which are among the most important reliability tests simulating environmental test conditions in display technologies, clearly shows that this TFT structure is suitable to use in display technologies in terms of long-term stability.

CHAPTER FIVE

CONCLUSIONS AND FUTURE PLANS

5.1 Conclutions

If it is necessary to summarize the results of this thesis, HfO_2 dielectric layer, $SrTiO_3$ buffer layer, IGZO semiconductor layer and ITO Srouce-Drain contacts were successfully produced by sputtering method on a flexible and transparent substrate, respectively. The flexible transparent TFT structure created has been subjected to the relevant environmental reliability tests and it has been shown that this TFT device produced after the tests works successfully. In addition, the application areas of new generation flexible transparent TFT structure developed in this thesis are clearly specified. The fabrication method developed within the scope of this thesis and the successful results obtained can be listed as follows:

1) HfO_2, $SrTiO_3$, IGZO and ITO materials were successfully produced as gate dielectric layer, buffer layer, semiconductor layer and Source-Drain contacts of the TFT structure, respectively, on ITO-coated PET substrate by sputtering method. During the production of all layers, the base pressure is 3.00x10-6 Torr and process vacuum level is 10mToor. RF power power is set as 60W, 50W, 25W and 30W for HfO_2, $SrTiO_3$, IGZO and ITO materials, respectively. The ability to use the same production system and method in the fabrication of all layers will provide a great advantage for the mass production stage of the relevant TFT device.

2) XRD is one of the important analysis used to validate the production method. The XRD results of the HfO_2, $SrTiO_3$ and IGZO layers that form the TFT structure have clearly shown that these layers can be produced in amorphous structure. None of these layers have grain boundaries, since each of the relevant layers is produced in an amorphous structure. This especially reduced the possibility of trapping electrons moving in this region between the dielectric layer and the semiconductor layer.

In addition, the ability to produce these layers in amorphous form allows them to be produced in large areas with ultra-low surface roughness.

3) XPS is an important surface analysis method used to show that the relevant layers can be produced at the desired chemical stoichiometry. The XPS results of the HfO_2, $SrTiO_3$ and IGZO layers clearly showed that these layers were produced at the correct stoichiometry. It is known that the differences in the chemical stoichiometry of the relevant layers will directly affect the electrical performance of the relevant TFT structure. In this context, the XPS results clearly show the success of the production method preferred in this thesis study.

4) It is known that electrons in the TFT structure move at the interface between the dielectric layer and the semiconductor layer. Therefore, the surface morphology and surface roughness of this region are very important for the electrical performance of the TFT device. The surface morphology of the HfO_2 and $SrTiO_3$ layers directly affects the surface morphology of the region between the dielectric layer and the semiconductor layer. AFM analysis results show that the average surface roughness values of both the HfO_2 layer and the HfO_2+$SrTIO_3$ structure are below 2 nm. Especially based on the studies in the literature, it is clearly seen that this value will not have a negative effect on the superior electrical performance of the relevant TFT structure.

5) Especially for a transparent TFT structure that application area is display technologies, how much light it passes in the visible area is very important. In this context, optical transmittance measurements show that this developed TFT structure has an average of 79% optical transmittance in the 400-700nm range. When this value is compared with the studies in the literature, it is clearly seen that it is at an acceptable level for transparent electronic applications.

6) The target application area of the TFT structure developed in this thesis is display technologies. In display technologies, it is very important in long-term stability as well as performance. In this context, IGZO, an AOS, has been preferred as a semiconductor layer in order to ensure stable operation of the relevant TFT structure in the long term. In order to test the long-term stability of the relevant structure, the TFT device has been put into TCT, TST and HTHH tests, which are frequently used for display applications. Before and after these environmental tests, the electrical performance of the relevant TFT structure was tested.

7) The unmodified TFT structure between the dielectric layer and the semiconductor layer was produced with 5 different channel geometries. The average fet mobility value of the developed TFT devices was calculated as 20.14 cm^2/Vs. The TFT structure having biggest channel geometry was preferred for surface modification, since the TFT with the widest channel geometry has the best reproducibility. The surface modification process of the HfO_2 dielectric layer was carried out with the $SrTiO_3$ layer with different thicknesses. Before environmental tests in the relevant TFT structure, the fet mobility value could be increased from 20.27 cm^2/Vs to 26.82 cm^2/Vs. The electrical characterization results clearly show that the interface modification process between the dielectric layer and the semiconductor layer increases the electrical performance of the relevant TFT structure.

8) As is known, electrons in TFT structures move at the interface between the semiconductor and the dielectric layer. The presence of oxygen atoms that do not bond with metal atoms at interface causes electrons to be trapped by unbound oxygen atoms. The electronegativity of Ti atoms, especially in $SrTiO_3$, which is preferred for surface modification, is better than the electronegativity of Hf atoms in HfO_2. This allows the metal atoms in $SrTiO_3$ to bond stronger and more with the O atoms in IGZO. Thus, at the interface, the number of metal atoms that have not bonded with the O atom in IGZO after surface modification decreases.

In this case, it reduces the possibility of the electrons being trapped at the interface by being attracted by O atoms that have not bonded. Thus, the fet mobility value of the TFT device related to surface modification could also be increased. In this thesis, one of the important analysis methods used to explain the increase in electrical performance obtained by surface modification, described above, is the XPS depth analysis method. The results of the XPS depth analysis clearly show that the number of oxygen atoms that have not bonded with metal atoms at the interface decreases as a result of surface modification.

9) The TFT device, that surface has been modified and has the highest fet mobility value, has been subjected to environmental tests. After environmental tests, electrical characterization processes were repeated on the relevant TFT structure. While the fet mobility value of the relevant TFT device was 26.82 cm2/Vs before environmental tests, this value decreased to 26.27 cm2/Vs after environmental tests. Considering that the relevant environmental test conditions have highly heavy conditions for long-term use on many devices to be used in consumer electronics, this negligible decrease in the fet mobility value of the relevant TFT device clearly shows that this TFT structure will provide long-term stability.

5.2 Future Plans

At the end of this thesis, the usability of the TFT device in new generation screen technologies has been clearly shown. In this context, the roadmap determined for the adaptability of the relevant TFT device to innovative TV or VS (Visual Solution) products and at the same time improving the electrical performance for the application is shared below.

- Testing different substrates for foldable TV applications in TFT production
- Testing the electrical performance of TFT for different folding angles
- Modification of the relevant TFT for buttom-top gate dielectric structure in order to compensate and correct the shifts in TFT's transfer characteristics over time
- Development of photolithography processes for smaller channel geometry
- Development of the sputtering production process that can coat the entire surface of a minimum 10.4 inch tablet screen
- Modification / testing of related photolithography and sputtering processes to produce TFT structures capable of driving pixels with HD (1280x720 pixels) resolution
- Applying for the licensing of the related TFT production process to a panel manufacturer with VESTEL Elektronik for the new method developed.

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